IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF WISCONSIN

SEMICONDUCTOR ENERGY LABORATORY CO., LTD., Plaintiff and Counter-Defendant, v. SAMSUNG ELECTRONICS CO., LTD., S-LCD CORPORATION, SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA, LLC, AND SAMSUNG MOBILE DISPLAY, CO. LTD., Defendants and Counterclaimants.	CIVIL ACTION NO. 3:09-CV-00001 JUDGE: Barbara B. Crabb **RULE 26(a)(2) EXPERT REPORT OF JAMES T. CARMICHAEL**

RULE 26(a)(2) EXPERT REPORT OF JAMES T. CARMICHAEL

I. GENERAL INTRODUCTION

A. Qualifications

1. My education and experience are summarized in the curriculum vitae attached hereto as **Exhibit 1**.

2. Upon graduating from Yale University with a Bachelor of Arts degree in 1984, I enrolled in the University of Wisconsin to study both electrical engineering and law concurrently. During college, I had a job one summer as a computer programmer at State Farm Insurance Co. While attending law school, I took a number of courses in the electrical engineering department. In 1987, I received a Juris Doctor degree from the University of Wisconsin, graduating with honors (cum laude). I later enrolled in the Master of Science in Electrical and Computer Engineering program at George Mason University. I completed about ten of the twenty courses required for that degree before leaving the program in 1996.

3. From 1987 to 1990, I was an associate attorney with Lyon & Lyon LLP, a large patent law firm based in Los Angeles, California. As an associate, I assisted in patent prosecution and litigation in various technologies such as microprocessors.

4. In 1990, I became the sole law clerk for Circuit Judge Howard T. Markey at the United States Court of Appeals for the Federal Circuit. In that role, I assisted Judge Markey in drafting opinions and discussing pending cases with the other Federal Circuit judges.

5. In 1991, I took and passed the examination for registration to practice in patent cases before the United States Patent and Trademark Office (the "Patent bar exam").

6. From 1991 to 1996, I was an attorney in the Office of the Solicitor at the United States Patent and Trademark Office ("USPTO").

7. In the Solicitor's Office, I was appointed coordinator of enrollment and disciplinary proceedings. In that role, I assigned and supervised all enforcement proceedings

against registered patent attorneys charged with violating the USPTO Code of Professional Responsibility. The issues in these matters included violation of attorneys' duty of candor and the duty to disclose information known to be material under 37 C.F.R. § 1.56 ("Rule 56"). See 37 C.F.R. § 10.23(c)(10). My official duties included evaluating hundreds of patent applications for possible intentional violation of the duty of candor and good faith under Rule 56.

8. I also assisted the USPTO in developing and issuing federal regulations. For example, I consulted with my then-colleagues in the Solicitor's Office in helping to develop the USPTO's 1992 revision of Rule 56. The regulation was modified at that time to emphasize that patent applicants have a duty of candor and good faith which is even broader than their duty to disclose material information to the USPTO. We also analyzed the standard of materiality applicable to the duty of disclosure. The resulting regulation (Rule 56) will be discussed in greater detail below.

9. As an Associate Solicitor, I helped revise sections of the Manual of Patent Examining Procedure ("MPEP"). I was responsible for legal review of MPEP Chapter 2000 (Duty of Disclosure), among others. Other duties included helping train groups of USPTO employees on proper procedures and ethics.

10. While in the Solicitor's Office, I briefed and argued approximately thirty appeals at the U.S. Court of Appeals for the Federal Circuit in cases involving patentability and USPTO procedure. I also represented the Commissioner of Patents and Trademarks in United States District Courts.

11. In 1996, I was appointed Examiner-in-Chief (also known as Administrative Patent Judge) in the Electrical division of the Board of Patent Appeals and Interferences. In that post, which I held until 1999, I was responsible for hearing and deciding appeals taken from final

rejections imposed by patent examiners regarding electrical inventions. In each case, I evaluated the arguments of the USPTO examiner and the arguments of the patent applicant's attorney, weighed the evidence of record, and rendered a decision affirming or reversing the examiner's decision. My decisions were considered the final agency action and were directly appealable to the U.S. Court of Appeals for the Federal Circuit.

12. I also evaluated additional prior art that might be used to enter a new ground of rejection in the patent application on appeal. I sometimes formulated and entered a new ground of rejection against the claims under consideration, in addition to or instead of the examiner's grounds for rejection.

13. As an Examiner-in-Chief I analyzed several patent applications for possible rejection under the doctrine of prosecution laches. In those particular cases, we did not find prosecution laches.

14. As an Examiner-in-Chief, I authored over two hundred (200) decisions determining patentability, and participated as a panel member for about six hundred (600) more. While I employed in the Solicitor's Office, I evaluated many other applications, including reviewing hundreds of patent applications for potential attorney misconduct. In all, I evaluated over one thousand (1000) patent applications in my official capacity at the USPTO.

15. I completed my public service in 1999 and opened a Washington, D.C. office for Lyon & Lyon LLP, the same patent law firm I was with in the 1980's. I served as managing partner of that office until the firm closed nationwide in 2002. Most of my work for Lyon & Lyon related to patent applications for electrical inventions. I also served as the Secretary of the Association of Patent Law Firms. Currently, I am a principal in the Northern Virginia office of Miles & Stockbridge P.C., a law firm of approximately two hundred attorneys in the

Washington, D.C. area. I am admitted to the bars of California and Washington, D.C., and I am registered to practice in patent cases before the USPTO.

16. My current practice consists primarily of preparing and prosecuting patent applications for electrical and computer-related inventions in the USPTO. I also handle attorney misconduct proceedings, litigation, appeals, expert consulting, patent licensing, and opinions.

B. Prior Expert Testimony

17. Prior to the present case, I provided expert testimony by deposition and/or at trial in the cases listed in **Exhibit 1**.

C. Summary of Work Performed

18. I have been retained by O'Melveny & Myers LLP, counsel for the defendants Samsung Electronics Co., Ltd., S-LCD Corporation, Samsung Electronics America, Inc., Samsung Telecommunications America, LLC, and Samsung Mobile Display Co., Ltd. (collectively "Samsung"), to provide expert opinions with respect to USPTO patent practice and procedure as applied to procurement of U.S. Patent No. 6,900,463 ("the '463 Patent").

19. Among other things, I have been asked by Samsung to perform the following tasks:

- Provide background information regarding procedures and practices at the USPTO, including those relating to the patent application process and the duty of candor and good faith;
- Review and analyze the prosecution histories for the '463 Patent-in-suit and U.S. Patent No. 5,543,636 ("the '636 Patent");
- Analyze whether the inequitable conduct Dr. Yamazaki was found to have committed in connection with the '636 Patent had a necessary and immediate relation to the '463 Patent;
- Determine whether Dr. Yamazaki's inequitable conduct in obtaining the '636 Patent provided him with an advantage in prosecuting the '463 Patent Application before the USPTO;

- Analyze whether the issued ‘463 claims were presented after an unreasonable and unexplained delay under USPTO procedures in relation to prosecution laches; and

- To the extent Dr. Nagata’s signature on certain documents is shown to have been forged, provide information on applicable USPTO procedures and prosecution history.

20. This report sets forth the subject matter of the testimony I may give at trial. I am familiar with and am prepared to testify about the following:

- Patent practice and procedure in the USPTO;

- The application process for obtaining a patent;

- USPTO policies and procedures with regard to double patenting and correcting issued patents;

- USPTO policies and procedures concerning the duty of candor and good faith in obtaining a patent, including *inter alia* the duty to disclose to the USPTO information material to patentability, especially as applied to the ‘463 Patent;

- The promulgation and application by the USPTO of 37 C.F.R. § 1.56;

- The prosecution history of the ‘463 and ‘636 Patents;

- The relationship between Dr. Yamazaki’s inequitable conduct in procuring the ‘636 Patent, as found by the District Court for the Eastern District of Virginia and the U.S. Court of Appeals for the Federal Circuit, and the ‘463 Patent prosecution;

- USPTO procedures and practice relating to prosecution laches, especially as applied to the ‘463 Patent; and

- USPTO procedures and prosecution history in relation to purported signatures of Dr. Nagata.

21. I reserve the right to supplement and/or amend the opinions expressed herein in response to positions taken by experts or Semiconductor Energy Laboratory Co., Ltd. (“SEL”), including any expert on Patent Office prosecution, to amplify what is stated above, where necessary, and especially in view of information not presently known to me or new information presented by SEL or SEL’s experts prior to, or at trial, and to supplement this report should additional information be brought to my attention during the course of this proceeding. I also

reserve the right to testify about matters that may be: (1) raised on cross-examination, (2) raised in depositions, (3) raised in expert reports I may receive in the future, (4) necessary to rebut any other matters about which SEL's experts may testify at deposition or trial, and (5) otherwise raised at trial by counsel or this Court in relation to the matters set forth in this report concerning which I am qualified to testify. I may prepare demonstrative exhibits for trial to illustrate my opinions and the information contained in this report.

D. Compensation

22. I have been retained by OMM to act as an independent expert consultant and possible witness. For this work, Miles & Stockbridge is being compensated at my usual hourly rate, $675 per hour plus reimbursement for expenses incurred. Miles & Stockbridge adjusts its rates every year, typically in October.

23. My right to compensation from Miles & Stockbridge is in no way contingent upon the outcome of this case or any issue in it. Miles & Stockbridge's right to receive payment from Defendants for my services is in no way contingent upon the outcome of this case or any issue in it.

II. MATERIALS REVIEWED IN FORMULATING OPINIONS

24. In connection with formulating my opinions in this matter, I have reviewed the materials listed in **Exhibit 2** attached hereto. I understand that discovery is ongoing, and I reserve the right to supplement or revise my opinions based on information I may receive in the future.

III. SUMMARY OF OPINIONS

25. In light of my expertise in USPTO practice and procedure and my experience working at the USPTO, I have reviewed the indicated materials and may testify to the following opinions:

- This case includes allegations by Dr. Shunpei Yamazaki and his company, SEL, that Samsung infringes Dr. Yamazaki's '463 Patent covering certain transistors.

- In a prior case between the same parties, Dr. Yamazaki and SEL accused Samsung of infringing a different patent (the '636 Patent) covering similar subject matter. In that case, the U.S. District Court for the Eastern District of Virginia found that Dr. Yamazaki had committed inequitable conduct by intentionally deceiving the USPTO when acquiring the '636 Patent. That decision was affirmed by the U.S. Court of Appeals for the Federal Circuit.

- The inequitable conduct committed by Dr. Yamazaki in obtaining the '636 Patent, found by the District Court and affirmed by the Federal Circuit, had a necessary and immediate relationship to the '463 Patent involved in the present suit.

- Dr. Yamazaki's inequitable conduct in relation to the '636 Patent provided him with an advantage in securing and enforcing the '463 Patent.

- In obtaining the '463 Patent, Dr. Yamazaki essentially recaptured certain subject matter that had been covered by the tainted '636 Patent.

- When revising the '636 claims after the '636 Patent had already issued, Dr. Yamazaki continued his inequitable conduct and concealed the fact that he was simultaneously seeking similar claims in the '436 Patent application. Dr. Yamazaki successfully avoided receiving a rejection of the '463 Patent for double patenting over the '636 Patent. A double patenting rejection may have required Dr. Yamazaki to file a terminal disclaimer in the USPTO, thereby cutting off most of the remaining term of the '463 Patent.

- Dr. Yamazaki, Mr. Yamamoto, Mr. Ferguson, and Mr. Robinson breached their duties of candor and good faith to the USPTO during the prosecution of the '463 Patent Application. For instance, they concealed material information arising out of the *SEL I* litigation regarding the tainted '636 Patent, such as a Motion for Reconsideration and an accompanying affidavit. That information was inconsistent with positions that they took before the USPTO to obtain the '463 Patent. As another example, they failed to disclose material prior art of which they were aware to the examiner of the '463 Patent. Moreover, they buried the '636 Patent in such a manner that the '463 examiner would not review its claims for double patenting.

- Dr. Yamazaki's delay in presenting the issued '463 claims to the USPTO appears to be unreasonable and unexplained under USPTO procedures with respect to prosecution laches.

- To the extent Dr. Nagata's signature on a "Substitute Declaration" was forged, it was a breach of the duty of candor and good faith leading to issuance of the '463 Patent.

IV. BACKGROUND INFORMATION

A. The Patent Application Process

26. An inventor may obtain a U.S. Patent by submitting a patent application to the USPTO. The application must describe the invention sufficiently to enable one of ordinary skill in the art to practice the invention, and conform to other statutory requirements. To be patentable, the claimed invention must be new and non-obvious in light of certain previous technology ("prior art"). Prior art for a given patent application includes, among other things, any information published more than one year prior to filing the application, including patent applications published anywhere in the world, prior public use activity, on sale activity, public knowledge by others, and inventions by others in the United States.[1]

27. Only one patent is allowed for a given invention. Double patenting of the same invention is not proper. If an application claims an invention that is an obvious variant of an invention claimed in another known application or patent, it should be rejected for double patenting.

28. At the USPTO, an examiner is assigned to evaluate ("examine") the application. The assigned examiner reviews the patent application and evaluates whether it meets the above-noted requirements. In performing that examination, the examiner searches for prior art pertinent to patentability of the claims and studies the information as presented by the inventor in the specification. The examiner also reviews any statements regarding the prior art made by the inventor. In evaluating the patent vis-à-vis the prior art, the patent examiner uses the broadest reasonable interpretation of the claims consistent with the specification, which is a broader standard than a court may use in litigation. One reason for this broader standard is that during prosecution, claims can be amended and do not have the benefit of a presumption of validity. If

an examiner becomes aware of another patent or application with a common inventor or owner, the examiner may consider whether improper double patenting would be present.

29. The examiner either allows the application to issue as a patent or determines that the application should not issue in its present form and rejects one or more claims. The examiner presents this evaluation to the inventor in a written communication generally referred to as an "Office Action."

30. If an Office Action rejects claims as unpatentable, an inventor's response will typically amend the application and/or argue against the rejection. The examiner then reexamines the application in light of the attorney's response and issues another Office Action. In cases where the examiner finds that an application should be allowed to issue as a patent, a Notice of Allowance is issued. If an examiner makes a final rejection, the inventor may appeal to the Board of Patent Appeals and Interferences. In that case, the inventor and examiner both submit briefs to the Board and the Board renders a decision. This back-and-forth process is generally referred to as patent "prosecution."

31. The USPTO's official record of the examination and prosecution process is referred to as the "prosecution history." At the time the '463 Patent was applied for, the USPTO maintained the prosecution history of each application by placing paper copies in a cardstock file jacket (or "file wrapper"). Currently, the USPTO maintains prosecution histories electronically.

32. The USPTO receives hundreds of thousands of patent applications every year, with a limited number of examiners to evaluate them. Examiners are placed on a production schedule that limits the amount of time they can spend per application. For example, in 2001, patent examiners spent an average of only 18 cumulative hours per patent application disposed,

[1] Manual of Patent Examining Procedure ("MPEP") § 706.02.

from the time of receiving the patent application through the conclusion of all Office Actions and all necessary submissions by the attorney.[2]

33. Due to the limited amount of time an examiner has to examine a patent and review the prior art references submitted by the patent applicant, examiners rely on the patent applicants and their representatives to act with candor and good faith in dealing with the USPTO, as required by USPTO regulations. Thus, patent applicants are required and expected to disclose information known to them to be material to patentability. Material prior art is generally called to an examiner's attention by filing an Information Disclosure Statement ("IDS").

34. Patent applications and requests for certificates of correction are handled by the USPTO on an *ex parte* basis. No opposing party is allowed to participate.

B. <u>USPTO Procedures Relating to Double Patenting</u>

35. The USPTO examines pending patent applications for possible "double patenting" rejections, stemming from the requirement in 35 U.S.C. § 101 that the USPTO grant only "a" patent (not multiple patents) for an invention. The USPTO's stated policy for issuing double patenting rejections is to prevent the unjustified extension of patent exclusivity beyond the enforceable term of a patent:

> The doctrine of double patenting seeks to prevent the unjustified extension of patent exclusivity beyond the term of a patent. The public policy behind this doctrine is that:
>
> > The public should . . . be able to act on the assumption that upon the expiration of the patent it will be free to use not only the invention claimed in the patent but also modifications or variants which would have been obvious to those of ordinary skill in the art at the time the invention was made, taking into account the skill in the art and prior art other than the invention claimed in the issued patent.

[2] *See* Office of Mgmt. & Budget, Executive Office of the President, Budget of the United States Government, Fiscal Year 2004 40 (2003), *available at* http://www.whitehouse.gov/omb/budget/fy2004/pdf/PMA.pdf.

> *In re Zickendraht*, 319 F.2d 225, 232, 138 USPQ 22, 27 (CCPA 1963) (Rich, J. concurring). Double patenting results when the right to exclude granted by a first patent is unjustly extended by the grant of a later issued patent or patents. *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982).
>
> Before consideration can be given to the issue of double patenting, there must be some common relationship of inventorship and/or ownership of two or more patents or applications. Since the doctrine of double patenting seeks to avoid unjustly extending patent rights at the expense of the public, the focus of any double patenting analysis necessarily is on the claims in the multiple patents or patent applications involved in the analysis.[3]

36. One type of double patenting rejection is referred to as "obviousness type" double patenting. This type of rejection is used to prevent prolongation of a patent term by prohibiting claims in a second patent not patentably distinguishable from claims in a first patent.[4]

37. An obviousness-type double patenting rejection may be made when any claim in the application under examination is merely an obvious variation of an invention claimed in another application (or patent). The analysis parallels the requirements of a rejection for obviousness under 35 U.S.C. § 103.[5]

38. For obviousness-type double patenting, the USPTO instructs examiners that, when considering whether the invention defined in a claim of an application under examination is an obvious variation of the invention defined in another application (or patent), an examiner may use the specification of the other application for certain purposes. For example, the examiner may use the specification of the other application as a dictionary to learn the meaning of its claim terms. Further, the examiner may examine and consider the portions of the other specification which provide support for the claims in the other application. In particular, the USPTO instructs examiners that:

[3] MPEP § 804 (Sixth Ed., Rev. 2, July 1996, at 800-9).
[4] *Id.*

> When considering whether the invention defined in a claim of an application is an obvious variation of the invention defined in the claim of a patent, the disclosure of the patent may not be used as prior art. This does not mean that one is precluded from all use of the patent disclosure.
>
> The specification can always be used as a dictionary to learn the meaning of a term in the patent claim. *In re Boylan*, 293 F.2d 1017, 157 USPQ 370 (CCPA 1968). Further, those portions of the specification which provide support for the patent claims may also be examined and considered when addressing the issue of whether a claim in the application defines an obvious variation of an invention claimed in the patent. *In re Vogel*, 422 F.2d 438, 164 USPQ 619, 622 (CCPA 1970). The court in *Vogel* recognized "that it is most difficult, if not meaningless, to try to say what is or is not an obvious variation of a claim," but that one can judge whether or not the invention claimed in an application is an obvious variation of an embodiment disclosed in the patent which provides support for the patent claim. According to the court, one must first "determine how much of the patent disclosure pertains to the invention claimed in the patent" because only "[t]his portion of the specification supports the patent claims and may be considered." The court pointed out that "this use of the disclosure is not in contravention of the cases forbidding its use as prior art, nor is it applying the patent as a reference under 35 U.S.C § 103, since only the disclosure of the invention claimed in the patent may be examined.[6]

39. Additional prior art may be combined with the invention claimed in the other application (or patent) to arrive at a conclusion of obviousness for a claim under examination.[7]

40. If the application under examination was filed in the USPTO later than the other application (or patent), then only "one-way" obviousness is needed. "One-way" obviousness is where a claim under examination would have been obvious from the invention claimed in the other application (or patent):

[5] MPEP § 804, subsection II.B.1 (Sixth Ed., Rev. 2, July 1996, at 800-16).
[6] *Id.* (pp. 800-17).
[7] MPEP § 804, subsection II.B.1, form paragraphs 8.36 ("Rejection, Obviousness Type Double Patenting – With Secondary Reference(s)") and 8.37 ("Provisional Rejection, Obviousness Type Double Patenting – With Secondary References") (Sixth Ed., Rev. 2, July 1996, at 800-19).

a. *One-Way Obviousness*

> If the application is the later filed case or both are filed on the same day, only a one-way determination of obviousness is needed in resolving the issue of double patenting – i.e., whether the invention defined in a claim in the application is an obvious variation of the invention defined in a claim in the patent. If a claimed invention in the application is obvious over a claimed invention in the patent, there would be an unjustified timewise extension of the patent and an obvious-type double patenting rejection is proper. Unless a claimed invention in the application is obvious over a claimed invention in the patent, no double patenting rejection of the obvious-type is made, but this does not necessarily preclude a rejection based on nonstatutory, nonobvious double patenting.[8]

41. Even if the application under examination is the earlier filed application, one-way obviousness is sufficient to reject the application in the absence of a finding of administrative delay:

> Similarly, even if the application at issue is the earlier filed case, only a one-way determination of obviousness is needed to support a double patenting rejection, in the absence of a finding of administrative delay on the part of the Office causing delay in prosecution of the application at issue, the earlier filed case. However, if administrative delay in prosecution of the application at issue, i.e., the earlier filed case, on the part of the Office results in earlier issuance of a patent on the later filed application containing conflicting claims, a two-way determination of obviousness may be required to support a double patenting rejection.[9]

42. If the other application was filed later but issued earlier, "two-way" obviousness may be required when the applicant could not have filed the claims in a single application and there was administrative delay by the USPTO in the application under examination. Unless the record clearly shows administrative delay and that the applicant could not have avoided filing separate applications, the USPTO may issue a double patenting rejection under the "one-way" standard and shift the burden to the applicant to prove that a "two-way" standard is required:

[8] MPEP § 804, subsection II.B.1.a (Sixth Ed., Rev. 2, July 1996, at 800-17)
[9] *Id.*

b. *Two-Way Obviousness*

> If the patent is the later filed application, the question of whether the timewise extension of the right to exclude granted by a patent is justified or unjustified must be addressed. A two-way test is to be applied only when the applicant could not have filed the claims in a single application and there is administrative delay. *In re Berg*, 46 USPQ2d 1226 (Fed. Cir. 1998) ("The two-way exception can only apply when the applicant could not avoid separate filings, and even then, only if the PTO controlled the rates of prosecution to cause the later filed species claims to issue before the claims for a genus in an earlier application . . . In Berg's case, the two applications could have been filed as one, so it is irrelevant to our disposition who actually controlled the respective rates of prosecution."). In the absence of administrative delay, a one way test is appropriate. *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993) (applicant's voluntary decision to obtain early issuance of claims directed to a species and to pursue prosecution of previously rejected genus claims in a continuation is a considered election to postpone by the applicant and not administrative delay). Unless the record clearly shows administrative delay by the Office and that applicant could not have avoided filing separate applications, the examiner may use the one-way obviousness determination and shift the burden to applicant to show why a two-way obviousness determination is required.[10]

43. When examining one application for possible double patenting over the claims in another pending application (as opposed to in an issued patent), the USPTO designates the double patenting rejection as "provisional" because the other pending application has not yet issued as a patent.

44. The USPTO instructs examiners to enter the provisional double patenting rejection in both of the pending patent applications, not just the one under examination. For example, Examiner Note 9 to form paragraph 8.37 states in addition to making a provisional double patenting

[10] MPEP § 804.

rejection in the application under examination, "[a] provisional double patenting rejection should also be made in the conflicting application."[11]

45. Likewise, the USPTO instructs examiners to maintain the provisional double patenting rejection in both of the conflicting applications unless it becomes the only rejection remaining in one of the applications. When it is the only rejection remaining in one application, the provisional double patenting rejection is withdrawn in that application, and converted to a double-patenting rejection in the other application:

> The "provisional" double patenting rejection should continue to be made by the examiner in each application as long as there are conflicting claims in more than one application unless that "provisional" double patenting rejection is the only rejection remaining in one of the applications. If the "provisional" double patenting rejection in one application is the only rejection remaining in that application, the examiner should then withdraw that rejection and permit the application to issue as a patent, thereby converting the "provisional" double patenting rejection in the other application(s) into a double patenting rejection at the time the one application issues as a patent.[12]

46. An obviousness type double patenting rejection may generally be overcome by a terminal disclaimer. A terminal disclaimer disclaims the terminal portion of a patent term that would extend beyond the expiration of the other patent's term.

47. Another type of double patenting is referred to as nonobviousness-type double patenting:

> There are some unique circumstances where it has been recognized that another type of nonstatutory double patenting rejection is applicable even where the inventions claimed in two or more applications/patents are considered nonobvious over each other. These circumstances are illustrated by the facts before the court in *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968).[13]

[11] MPEP § 804, subsection II.B.1 (Sixth Ed., Rev. 2, July 1996, at 800-20).
[12] MPEP § 804, subsection I.B (Sixth Ed., Rev. 2, July 1996, at 800-14).
[13] MPEP § 804, subsection II.B.2 (Sixth Ed., Rev. 2, July 1996, at 800-20).

C. USPTO Procedures Concerning Prosecution Laches

48. Under USPTO procedures, a patent application may be rejected under the doctrine of prosecution laches due to an unreasonable and unexplained delay in prosecution. For example, where an applicant files multiple continuation applications over a period of time and does not substantively advance prosecution of the patent application, such a patent may be rejected under the doctrine of prosecution laches. However, it is unusual for the USPTO to become aware of circumstances that would justify rejecting a patent for prosecution laches.

D. USPTO Procedures Concerning Correcting An Issued Patent

49. If an error occurs in an issued patent, there are several possible procedures for correction by the USPTO. For example, a patentee may apply for a reissue patent where the error arose without deceptive intent and renders the patent wholly or partly invalid or inoperative:

> Errors in a patent may be corrected in four ways, namely (1) by reissue, (2) by the issuance of a certificate of correction which becomes a part of the patent, (3) by disclaimer, and (4) by reexamination.
>
> * * * * *
>
> Whenever any patent is, through error without any deceptive intention, deemed wholly or partly inoperative or invalid, by reason of a defective specification or drawing, or by reason of the patentee claiming more or less than he had a right to claim in the patent, the Commissioner shall, on the surrender of such patent and the payment of the fee required by law, reissue the patent for the invention disclosed in the original patent, and in accordance with a new and amended application, for the unexpired part of the term of the original patent. No new matter shall be introduced into the application for reissue.[14]

[14] MPEP § 1401 (Sixth Ed., Rev. 2, July 1996, at 1400-1).

50. An applicant in a reissue application is subject to the duty of candor and good faith.[15] Thus, a reissue application can be rejected if the underlying patent was obtained through inequitable conduct:

> Clearly, if a reissue patent would not be enforceable after its issue because of "fraud", "inequitable conduct" or "violation of the duty of disclosure" during the prosecution of the patent sought to be reissued, the reissue patent application should not issue. Under such circumstances, an appropriate remedy would be to reject the claims in the application in accordance with 35 U.S.C. § 251, see MPEP § 2022.05 and Chapter 1400.[16]

51. Second, certain errors by an applicant can be corrected pursuant to 35 U.S.C. § 255 and 37 C.F.R. § 1.323 by a Certificate of Correction if the error is of a minor character, would not require re-examination, and does not materially affect the scope or meaning of the patent:

> *35 U.S.C. 255. Certificate of correction of applicant's mistake.*
>
> Whenever a mistake of a clerical or typographical nature, or of minor character, which was not the fault of the Patent and Trademark Office, appears in a patent and a showing has been made that such mistake occurred in good faith, the Commissioner may, upon payment of the required fee, issue a certificate of correction, if the correction does not involve such changes in the patent as would constitute new matter or would require reexamination. Such patent, together with the certificate, shall have the same effect and operation in law on the trial of actions for causes thereafter arising as if the same had been originally issued in such corrected form.
>
> *37 CFR 1.323. Certificate of correction of applicant's mistake.*
>
> Whenever a mistake of a clerical or typographical nature or of minor character which was not the fault of the Office, appears in a patent and a showing is made that such mistake occurred in good faith, the Commissioner may, upon payment of the fee set forth in §1.20(a), issue a certificate, if the correction does not involve such changes in the patent as would constitute new matter or would require reexamination. A request for a certificate of correction of a patent involved in an interference shall comply with the

[15] MPEP § 2003 (Sixth Ed., Rev. 2, July 1996, at 2000-6).
[16] MPEP § 2012 (Sixth Ed., Rev. 2, July 1996, at 2000-10).

> requirements of this section and shall be accompanied by a motion under § 1.635.
>
> 37 CFR 1.323 relates to the issuance of Certificates of Correction for the correction of errors which were not the fault of the Office. A mistake is not of a minor character if the requested change would materially affect the scope or meaning of the patent.[17]

E. <u>Duty of Candor and Good Faith</u>

52. A patent by its very nature is affected with a public interest.[18] The public interest is best served, and the most effective patent examination occurs, when the USPTO is aware of and evaluates all material information.[19] Each person substantively involved with a patent application has a duty of candor and good faith toward the USPTO. This generally applies to the inventors, their attorneys, employees of the assignee, and anyone else that is substantively involved with the application. Because patents and certificates of correction are generally obtained *ex parte*, with no participation by anyone but the applicants, compliance with the duty of candor and good faith is important to prevent improper conduct before the USPTO. This is particularly important given that the USPTO has limited resources available to uncover information material to its decisions, and cannot generally question witnesses, search for litigation materials, or otherwise find out everything an inventor might know. This is compounded by the fact that examiners generally have a set amount of time they can average for each application.

53. The duty of candor and good faith is designed to provide the USPTO with the information necessary for effective and efficient decision making. Examiners and other USPTO personnel place great reliance on inventors to fulfill their duty of candor and good faith. Generally speaking, the USPTO accepts representations from inventors at face value and expects

[17] MPEP § 1481 (Sixth Ed., Rev. 2, July 1996, at 1400-64).
[18] 37 C.F.R. § 1.56(a).

that the duty of candor and good faith is being complied with. Examiners do not expect half-truths or misleading statements or representations from inventors. The over-arching duty of candor and good faith includes, among other things, a specific duty of disclosure.

54. The duty of candor is not merely a procedural requirement, but rather an affirmative duty on the part of those substantively involved with a patent application to disclose to the USPTO all information known or reasonably known to the applicants and their representative that is material to the patent application. This is because much of the information relevant to a given patent application is often known only by the applicants and their representatives. Thus, a patent applicant has a duty to disclose not only known and reasonably known prior art, but also other material information such as research conducted by the applicant, reverse engineering analyses of products, product literature and analyses and related litigation, among other materials.

55. The USPTO has promulgated a regulation to address the duty of candor and good faith, especially the duty of disclosure subsumed therein. That regulation, 37 C.F.R. § 1.56, is sometimes referred to as "Rule 56." The USPTO addresses the duty of candor and good faith in Chapter 2000 of the Manual of Patent Examining Procedure ("MPEP").[20] At the time the '463 Patent Application was submitted to the USPTO (September 8, 1992), I was responsible for legal review of Chapter 2000 in the USPTO Office of the Solicitor.

56. The Introduction to Chapter 2000 of the Manual currently states:[21]

> This Chapter deals with the duties owed toward the U.S. Patent and Trademark Office by the inventor and every other individual who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor or the inventor's assignee. These duties, of candor and good faith and

[19] 37 C.F.R. § 1.56(a).
[20] *See* MPEP § 2000 *et. seq.* (7th ed. 1998).
[21] MPEP § 2000.01 (Introduction) (7th ed. 1998).

> disclosure, have been codified in 37 CFR 1.56, as promulgated pursuant to carrying out the duties of the Director under Sections 2, 3, 131, and 132 of Title 35 of the United States Code.[22]

57. Section 2001.04 of the MPEP stated:

> The language of 37 CFR 1.56 (and 37 CFR 1.555) has been modified effective March 16, 1992 to emphasize that there is a duty of candor and good faith which is broader than the duty to disclose material information. 37 CFR 1.56 further states that "no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct."[23]

58. Both before and after 1992, Rule 56 required inventors to disclose to the USPTO all material information, including information likely to be important to a reasonable examiner (or other deciding official). Before 1992, Rule 56 stated in pertinent part:

> (a) A duty of candor and good faith toward the Patent and Trademark Office rests on the inventor, on each attorney or agent who prepares or prosecutes the application and on every other individual who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the invention. All such individuals have a duty to disclose to the Office information they are aware of which is material to the examination of the application. Such information is material where there is a substantial likelihood that a reasonable examiner would consider it important in deciding whether to allow the application to issue as a patent. The duty is commensurate with the degree of involvement in the preparation or prosecution of the application.
>
> (b) Disclosures pursuant to this section must be accompanied by a copy of each foreign patent document, non-patent publication, or other non-patent item of information in written form which is being disclosed or by a statement that the copy is not in the possession of the person making the disclosure and may be made to the Office through an attorney or agent having responsibility for the preparation or prosecution of the application or through an inventor who is acting in his or her own behalf. Disclosure to such

[22] MPEP § 2000 (Introduction) (7th ed. 1998).
[23] MPEP § 2001.04 (7th ed. 1998).

> an attorney, agent or inventor shall satisfy the duty, with respect to the information disclosed, of any other individual. Such an attorney, agent or inventor has no duty to transmit information which is not material to the examination of the application.[24]

59. Under the pre-1992 version of Rule 56, no patent would be granted in certain circumstances, such as where fraud was practiced or attempted on the USPTO:

> (d) No patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or gross negligence. The claims in an application shall be rejected if upon examination pursuant to 35 U.S.C. 131 and 132, it is established by clear and convincing evidence (1) that any fraud was practiced or attempted on the Office in connection with the application, or in connection with any previous application upon which the application relies, or (2) that there was any violation of the duty of disclosure through bad faith or gross negligence in connection with the application, or in connection with any previous application upon which the application relies.[25]

60. After 1992, the USPTO revised Rule 56 to state in pertinent part:

> (a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all

[24] 37 C.F.R. § 1.56 (1991) (Duty of disclosure; fraud; striking or rejecting applications).
[25] 37 C.F.R. § 1.56(d) (1991) (Duty to disclose information material to patentability).

information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

> (1) prior art cited in search reports of a foreign patent office in a counterpart application, and
>
> (2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.[26]

61. Post-1992 Rule 56 also defined material information as follows:

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

> (1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or
>
> (2) It refutes, or is inconsistent with, a position the applicant takes in:
>
> > (i) Opposing an argument of unpatentability relied on by the Office, or
> >
> > (ii) Asserting an argument of patentability.

A *prima facie* case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.[27]

* * * * *

[26] 37 C.F.R. § 1.56(a) (2007).

> (e) In any continuation-in-part application, the duty under this section includes the duty to disclose to the Office all information known to the person to be material to patentability, as defined in paragraph (b) of this section, which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.[28]

62. Additionally, post-1992 Rule 56 identified those who owe a duty of candor related to the filing of a patent application:

> (c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:
>
> (1) Each inventor named in the application;
>
> (2) Each attorney or agent who prepares or prosecutes the application; and
>
> (3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.
>
> (d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.[29]

63. Thus, the post-1992 version of Rule 56 provides specific examples of information that would be considered likely to be important to a reasonable examiner under the pre-1992 standard, and emphasizes that patent attorneys should carefully examine prior art cited by a foreign patent office in a counterpart application.

64. A failure to disclose all known information material to patentability would breach the inventor's duty of disclosure and may render a patent unenforceable.

65. As noted above, the over-arching duty of candor and good faith is broader than the duty of disclosure, and may be breached by submitting information that applicants knew or

[27] 37 C.F.R. § 1.56(b) (2007).
[28] 37 C.F.R. § 1.56(c-e) (2007) (Section (e) was added effective November 7, 2000).

should have known would mislead the USPTO. For example, submitting a forged document would generally be a violation of the duty of candor and good faith.

66. USPTO Rule 1.4 requires that each piece of correspondence required to be signed, such as an Assignment, be personally signed in permanent ink by the person whose name appears.[30] Presenting a paper to the USPTO constitutes a certification that the statements in the paper are made with the knowledge that whoever makes any false representations, or makes or uses any false writing or document, shall be subject to criminal penalties and that violation may jeopardize the enforceability of a related patent.[31]

67. While I was working at the USPTO as coordinator of attorney disciplinary proceedings, I personally prosecuted a disciplinary proceeding against a practitioner for submitting documents bearing his signed name but which were not actually signed by him. During administrative proceedings, I employed the assistance of a handwriting expert from the Federal Bureau of Investigation to prove that the signatures were not genuine. The practitioner was suspended from practice before the USPTO and was never reinstated. Submitting forged signatures to the USPTO is considered a serious violation of the duty of candor and good faith and may result in the patent being held unenforceable.

68. In some instances, a rejection over a reference can be overcome by showing that the reference was commonly owned at the time the claimed invention was made. The showing may include an executed assignment. The USPTO accepts such representations because of a heavy reliance on the applicant's duty of candor and good faith:

> The applicant(s) or the representive(s) of record have the best knowledge of the ownership of their application(s) and references(s), and their statement of such is sufficient evidence

[29] 37 C.F.R. § 1.56(c-d) (2007).
[30] 37 C.F.R. § 1.4(d).
[31] 37 C.F.R. § 11.18(b) (previously 37 C.F.R. § 10.18).

> because of their paramount obligation of candor and good faith the USPTO.[32]

69. A submitted assignment is required to be signed by the person purportedly giving the assignment. Knowingly preparing or submitting a forged assignment would violate the duty of candor and good faith.

70. The USPTO has also recognized a duty of reasonable inquiry for applicants to investigate when they should have known that material information existed.[33] Without that, an applicant could deceive the USPTO by turning a blind eye and remaining willfully ignorant. The MPEP further advises that, when in doubt, it is desirable and safest to submit information.[34]

71. In my personal experience, the USPTO often has no way to know that the duty of candor and good faith has been violated or that an inventor has withheld material information.

72. Occasionally, such violations are detected in the course of investigating a registered patent attorney accused of misconduct or in prosecuting such attorneys for disbarment or other discipline. While working at the USPTO Office of the Solicitor, I was coordinator of attorney discipline proceedings at the time the '463 Patent Application was filed. In that role, I investigated hundreds of applications to evaluate whether there had been an intentional violation of the duty of candor and good faith under Rule 56.

73. The vast majority of patent applications and requests for certificates of correction handled by the USPTO are not subject to such scrutiny. This is because the USPTO processes hundreds of thousands of applications every year, and such scrutiny of every patent application is not feasible.

[32] MPEP § 706.02(l)(2).
[33] MPEP § 2001.02 (Fifth Ed., Rev. 3, May 1986 at 2000-4).
[34] MPEP § 2001.04.7 (Sixth Ed., Rev. 2, July 1996 at 2000-8).

74. In my investigations, I determined that the duty of candor and good faith was extremely important for ensuring the integrity of the patent process. Otherwise, it could be relatively easy in some circumstances to obtain a patent or other favorable USPTO decision through withholding material information or submitting misleading information, with little chance of detection by the USPTO. My investigations revealed that it had been done many times. Someone who is determined enough may be able to obtain hundreds of patents through such deceit.

1. USPTO Procedures Regarding The Duty To Disclose Information From Other Applications

75. USPTO procedures impose on applicants a duty to disclose material information. This includes material information from co-pending patent applications. Information is material where there is a substantial likelihood that a reasonable examiner would consider it important in deciding whether to allow the application.[35] As detailed above, information that establishes, by itself or in combination with other known information, a *prima facie* case of unpatentability of a claim may be one example.[36]

76. If an inventor has two applications claiming different but patentably indistinct subject matter, that fact must be brought to the attention of the examiner in both applications:

> The individuals covered by 37 CFR 1.56 have a duty to bring to the attention of the examiner, or other Office official involved with the examination of a particular application, information within their knowledge as to other copending United States applications which are "material to the patentability" of the application in question. As set forth by the Court in *Armour & Co. v. Swift & Co.*, 175 USPQ 70, 79 (7th Cir. 1972),
>
> > "we think that it is unfair to the busy examiner, no matter how diligent and well informed he may be, to assume that he retains details of every pending file in his mind when he

[35] MPEP § 2001.05 (Fifth Ed., Rev. 13, November 1989 at 2000-5).
[36] MPEP § 2001.05 (Sixth Ed., Rev. 3, July 1997 at 2000-4) (Materiality Under 37 CFR 1.56)).

> is reviewing a particular application…[T]he applicant has the burden of presenting the examiner with a complete and accurate record to support the allowance of letters patent."
>
> Accordingly, the individuals covered by 37 CFR 1.56 cannot assume that the examiner of a particular application is necessarily aware of other applications "material to patentability" of the application in question, but must instead bring such other applications to the attention of the examiner. For example, if a particular inventor has different applications pending in which similar subject matter but patentable distinct claims are present that fact must be disclosed to the examiner of each of the involved applications. Similarly, the prior art references from one application must be made of record in another subsequent application if such prior art references are "material to patentability" of the subsequent application.[37]

77. "Patentably indistinct" generally refers to claimed inventions that could be considered directed to the same invention or to obvious variations.

78. A patentably indistinct claim in another application or patent would generally be material at least because it could support a *prima facie* case of unpatentability for double patenting in the absence of a terminal disclaimer.

79. The MPEP cautions applicants not to rely on an examiner to be aware of other applications belonging to the same applicant.[38] Indeed, applicants are advised that it is desirable to call co-pending applications to the attention of the examiner even if there is only a question that they might be material.[39] Moreover, the MPEP tells applicants not to assume that an examiner will necessarily remember, when examining a particular application, other applications which the examiner is examining, or has examined in the past.[40] A lapse on the part of the USPTO in identifying such information does not excuse the applicant.[41]

[37] MPEP § 2001.06(b) (Sixth Ed, Rev. 3, July 1997 at 2000-5) (internal citations omitted).
[38] MPEP § 2001.04 (Sixth Ed., Rev. 2, July 1996, at 2000-8).
[39] *Id.*
[40] *Id.*
[41] *Id.*

2. USPTO Procedures Regarding The Duty to Disclose Litigation Materials

80. USPTO procedures require patent applicants to disclose material information regardless of the source:

> All individuals covered by 37 CFR 1.56 (reproduced in MPEP § 2001.01) have a duty to disclose to the Patent and Trademark Office all material information they are *aware* of regardless of the source of or how they became aware of the information. Materiality controls whether information must be disclosed to the Office, not the circumstances under which or the source from which the information is obtained. If material, the information must be disclosed to the Office. The duty to disclose material information extends to information such individuals are aware of prior to or at the time of filing the application or become aware of during the prosecution thereof.
>
> Such individuals may be or become aware of material information from various sources such as, for example, co-workers, trade shows, communications from or with competitors, potential infringers, or other third parties, related foreign applications (see MPEP § 2001.06(a)), prior or copending United States patent applications (see MPEP § 2001.06(b)), related litigation (see MPEP § 2001.06(c)) and preliminary examination searches.[42]

81. As discussed above, material information is not limited to prior art, but instead embraces any information that would be important to a "reasonable examiner" in deciding whether or not to allow the application.[43] This includes information inconsistent with a position taken by an applicant in opposing an argument of unpatentability relied on by the USPTO,[44] as well as information from related litigation:

> Where the subject matter for which a patent is being sought is or has been involved in litigation, the existence of such litigation and any other material information arising therefrom must be brought to the attention of the Patent and Trademark Office; such as, for

[42] MPEP § 2001.06 (Sixth Ed, Rev. 3, July 1997 at 2000-4).
[43] MPEP § 2001.05 (Fifth Ed., Rev. 13, November 1989 at 2000-5); 37 C.F.R. § 1.56; MPEP § 2001.06 (Sixth Ed, Rev. 3, July 1997 at 2000-4).
[44] MPEP § 2001.05 (Sixth Ed., Rev. 3, July 1997 at 2000-4).

> example, evidence of possible prior public use or sales, questions of inventorship, prior art, allegations of "fraud," "inequitable conduct," or violation of duty of disclosure. Such information might arise during litigation in, for example, pleadings, admissions, discovery including interrogatories, depositions, and other documents, and testimony.[45]

V. THE '636 PATENT

A. Claim of Priority

82. On May 18, 1984, SEL filed Japanese Patent Applications 59-100250 ("the '250 Application"), 59-100251 ("the '251 Application"), and 59-100252 ("the '252 Application"), which were published as Japanese Unexamined Patent Application Publications 60-245172, 60-245173, and 60-245174 on December 4, 1985. The '250, '251, and '252 Japanese Applications named as an inventor Dr. Yamazaki. The '636 Patent claims priority to Japanese Application Nos. '250, '251, and '252.

83. On May 20, 1985, SEL filed U.S. Patent Application No. 06/735,697 ("the '697 Application"), which is now abandoned. On February 3, 1988, SEL filed U.S. Patent Application No. 07/153,477 ("the '477 Application"), which is a continuation of the '697 Application and which issued as U.S. Patent No. 4,959,700 on September 25, 1990. On May 9, 1990, SEL filed U.S. Patent Application No. 07/520,756 ("the '756 Application"), which is a divisional of the '477 Application and which is now abandoned. On May 24, 1991, SEL filed U.S. Patent Application No. 07/707,178 ("the '178 Application"), which is a continuation of the '756 Application and which issued as U.S. Patent No. 5,142,344 on August 25, 1992. On May 19, 1992, SEL filed U.S. Patent Application No. 07.885,643 ("the '643 Application"), which is a divisional of the '178 Application and which is now abandoned. On December 8, 1992, SEL filed U.S. Patent Application No. 07/987,179 ("the '179 Application") which is a

[45] MPEP§ 2001.06(c) (Sixth Ed, Rev. 3, July 1997 at 2000-5).

divisional of the '643 Application and which issued as U.S. Patent No. 5,315,132 on May 24, 1994. On March 18, 1994, SEL filed U.S. Patent Application No. 08/214,494 ("the '494 Application"), which is a divisional of the '179 Application and which is now abandoned. On April 20, 1995, SEL filed U.S. Application No. 08/425,455 ("the '455 Application"), which is a continuation of the '494 Application and which is now abandoned.

84. The application that eventually matured into the '636 Patent was filed by SEL on June 7, 1995. This application, U.S. Patent Application No. 08/473,953 ("the '953 Application"), which is a divisional of the '455 Application, is entitled "Insulated Gate Field Effect Transistor," and issued on August 6, 1996.[46] The '636 Patent identifies Dr. Yamazaki as a named inventor.

B. Prosecution History of the '636 Patent

1. Originally-Filed Claims

85. The originally-filed patent application contained two independent claims and five dependent claims. Exemplary Claim 1 recited the following limitations:

> 1. An insulated gate field effect transistor comprising:
>
> a high resistivity semiconductor layer formed on a substrate having an insulating surface;
>
> a gate electrode formed on the semiconductor layer with a gate insulating layer sandwiched therebetween in a manner to separate the semiconductor layer into two as viewed from above; and
>
> N- or P-type source and drain regions formed in first and second regions of the semiconductor layer on both sides of the gate electrode, as viewed from above, to extend vertically from the upper surface of the first and second regions toward the substrate in such a manner that the source and drain regions define therebetween a channel forming region, the source and drain regions being lower in resistivity than the channel forming region;
>
> wherein the semiconductor layer is constituted of a non-single-

[46] *See* the '636 Patent family tree, attached hereto as **Exhibit 3**.

crystal semiconductor doped with a recombination center neutralizer, and accordingly, the channel forming region is constituted of the non-single-crystal semiconductor doped with the recombination center neutralizer; and

wherein source-side and drain-side crystallized regions of a higher degree of crystallization than the channel forming region and doped with the recombination center neutralizer are respectively formed in the first and second regions of the semiconductor layer to extend vertically from the supper surface thereof.

2. Preliminary Amendment Dated 6/7/95

86. On June 7, 1995, SEL filed a Preliminary Amendment in which it amended its claim of priority with the following statement:

> This is a Divisional application of Serial No. 08/425,455, filed April 20, 1995; which itself is a continuation of Serial No. 08/214,494, filed March 18, 1994, now abandoned; which itself is a division of Serial No. 07/987,179, filed December 8, 1992, now U.S. Patent 5,315,132; which is a division of Serial No. 07/885,643, filed May 19, 1992, abandoned; which is a division of Serial No. 07/707,178, filed May 24, 1991, now U.S. Patent 5,142,344; which is a continuation of Serial No. 07/520,756, filed May 9, 1990, abandoned; which is a division of Serial No. 07/153,477, filed February 3, 1988, now U.S. Patent4,959,700; which is a continuation of Serial No. 06/735,697, filed May 20, 1985, abandoned.

87. SEL further cancelled Claim 1 and substituted new Claims 8-12, all of which were independent claims. Claims 8-12 recited the following limitations:

> 8. An insulated-gate field effect transistor comprising:
>
> a non-single crystalline semiconductor layer doped with a hydrogen or halogen and having a conductivity type selected from the group consisting of n-, p-, and intrinsic types;
>
> a channel region formed in said semiconductor layer, wherein a concentration of at least one of oxygen, carbon and nitrogen in said semiconductor layer is not higher than $5x10^{18}$ atoms/cm^3;
>
> source and drain regions contacting said channel region;
>
> a gate insulator comprising silicon nitride and directly contacting said channel region; and

a gate electrode contacting said gate insulator;

wherein said channel region is interposed between the gate `insulator and another insulator.

9. An insulated-gate filed effect transistor comprising:

a non-single crystalline semiconductor layer doped with a hydrogen or halogen and having a conductivity type selected from the group consisting of n-, p-, and intrinsic types;

a channel region formed in said semiconductor layer, wherein a concentration of at least one of oxygen, carbon and nitrogen contained in at least a portion of said channel region is not higher than $5x10^{18}$ atoms/cm^3;

source and drain regions contacting said channel region;

a gate insulator comprising silicon nitride and directly contacting said channel region; and

a gate electrode contacting said gate insulator;

wherein said channel region is interposed between the gate insulator and another insulator.

10. A thin film transistor comprising:

a non-single crystalline semiconductor layer doped with a hydrogen or halogen and having a channel region disposed in the semiconductor layer;

source and drain regions in contact with said channel region where the channel region is disposed between said source and drain regions,

a gate insulating film comprising silicon nitride and directly contacting said channel region; and

a gate electrode contacting said gate insulating film;

wherein at least a portion of said channel region contains oxygen in an amount not exceeding $5x10^{18}$ atoms/cm^3;

wherein said channel region is interposed between the gate insulating film and another insulator.

11. A thin film transistor comprising:

a non-single crystalline semiconductor layer doped with a hydrogen or halogen and having a channel region disposed in the semiconductor layer;

source and drain regions in contact with said channel region where the channel region is disposed between said source and drain regions,

a gate insulating film comprising silicon nitride and directly contacting said channel region; and

a gate electrode contacting said gate insulating film;

wherein at least a portion of said channel region contains nitrogen in an amount not exceeding $5x10^{18}$ atoms/cm^3;

wherein said channel region is interposed between the gate insulating film and another insulator.

12. A thin film transistor comprising:

a non-single crystalline semiconductor layer doped with a hydrogen or halogen and having a channel region disposed in the semiconductor layer;

source and drain regions in contact with said channel region where the channel region is disposed between said source and drain regions,

a gate insulating film comprising silicon nitride and directly contacting said channel region; and

a gate electrode contacting said gate insulating film;

wherein at least a portion of said channel region contains carbon in an amount not exceeding $5x10^{18}$ atoms/cm^3;

wherein said channel region is interposed between the gate insulating film and another insulator.

3. Supplemental Information Disclosure Statement Dated 8/10/95

88. On August 10, 1995, SEL filed a Supplemental Information Disclosure Statement in which it informed the Examiner that a "copending application Serial No. 08/470,599 is directed to subject matter related to that of the ['953 Application]."

4. Examiner Interview Dated 9/28/95

89. On September 28, 1995, Mr. Gerald Ferguson, Dr. Yamazaki, Mr. Dave Ostrowski and Ms. Teresa Arroyo attended an interview with the examiner, Mrs. Valencia Martin Wallace, regarding the '953 Application. The Examiner Interview Summary Record indicates that the attendees discussed changes to Claims 8-12 of the '953 Application that would make the claims "basically the same as in [U.S. Patent Application No. 08/425,455], which has been allowed." The notes also indicate that SEL agreed to file a terminal disclaimer, Information Disclosure Statement, and preliminary amendment for the '953 Application, "limiting the gate insulator to silicon nitride or silicon and nitrogen layers."

5. Preliminary Amendment, Terminal Disclaimer, and Information Disclosure Statement Dated 11/15/95

90. On November 15, 1995, SEL filed a Preliminary Amendment, Terminal Disclaimer and Information Disclosure Statement. The Information Disclosure Statement submitted additional prior art references known to the applicant and requested that the additional references be made of record in the '953 Application. The submitted prior art references included U.S. Patent Nos. 4,460,670, 4,418,132, 4,420,872, 4,690,717, 4,889,782, and 4,889,783, and Japanese Patent Laid-Open Nos. 4-49,269, 55-011329, 55-029154, 55-50,663, 55-50,664, 57-13,777, 58-92,217, 58-155773, and 58-161380. SEL also cited additional publications, including Matsumura, Japanese Journal of Applied Physics, *(Invited) Amorphous Silicon Transistors and Integrated Circuits*, 1983, P.G. LeComber, Electronics Letters,

Amorphous-Silicon Field-Effect Device and Possible Applications, 3/15/79, and K. Roy, *IEEE Electronic Device Letters* 1980, and Affidavit of Chuang Chuang Tsai. SEL also provided an explanation of certain prior art references, including the following references: Japanese Patent Laid-Open Nos. 55-011329, 55-029154, 58-155773, 58-155774, 58-161380, 59-35488, 56-135968, 55-50663, 55-50664, 57-13,777 and 56-245968. SEL further provided a partial translation of Japanese Patent Laid-Open No. 56-135968 ("the Japanese '968 Patent") and references that were noted in a Japanese Opposition against the Japanese '968 Patent, and a brief description of the contents of the Japanese '968 Patent.

91. SEL also amended its claim of priority with the following statement, and noted that many of the references in the newly cited applications should have been considered by the Examiner:

> Serial No. 735,697 included another divisional application, Serial No. 06/912,498, which issued as U.S. Patent No. 4,727,044. Furthermore, Serial No. 07/885,643 included another divisional application, Serial No. 07/987,160 filed December 8, 1992 (now abandoned), which included a continuation application, Serial No. 08/386,187 filed February 9, 1995 (currently pending), and the '643 application also included a continuation application, Serial No. 08/171,769 filed December 22, 1993 (currently being appealed). Additionally, Serial No. 987,179 included another divisional application, Serial No. 08/214,550 filed March 18, 1994 (now abandoned), which included a continuation application, Serial No. 08/426,487 filed April 20, 1995 (currently pending).

92. In its Terminal Disclaimer, SEL specifically disclaimed the terminal part of the statutory term of any patent granted on the '953 Application which would extend beyond the expiration date of the full statutory term, as shortened by any disclaimer, of the '132 Patent.

93. In the Preliminary Amendment SEL cancelled Claims 2-7, amended Claims 8-12 and added new Claims 13-17. Amended Claims 8-12 and new Claims 13-17 were all independent claims. Amended Claims 8-12 recited the following limitations:

8. An insulated gate field effect transistor comprising:

a non-single crystalline semiconductor layer doped with a hydrogen or halogen and having an intrinsic conductivity type [selected from the group consisting of n-, p-, and intrinsic types];

a channel region formed in said semiconductor layer, wherein a concentration of at least one oxygen, carbon and nitrogen contained in said semiconductor layer is not higher than $5x10^{18}$ atoms/cm^3;

source and drain regions [contacting] forming respective junctions with said channel region whereby charge carriers move through said channel region between said source and drain regions in a path substantively parallel to said substrate;

a gate insulator comprising silicon nitride and directly contacting said channel region; and

a gate electrode contacting said gate insulator;

wherein said channel region is interposed between the gate insulator and another insulator.

9. An insulated-gate filed effect transistor comprising:

a non-single crystalline semiconductor layer doped with a hydrogen or halogen and having an intrinsic conductivity type [selected from the group consisting of n-, p-, and intrinsic types];

a channel region formed in said semiconductor layer, wherein a concentration of at least one of oxygen, carbon and nitrogen contained in at least a portion of said channel region is not higher than $5x10^{18}$ atoms/cm^3;

source and drain regions [contacting] forming respective junctions with said channel region whereby charge carriers move through said channel region between said source and drain regions in a path substantially parallel to said substrate;

a gate insulator comprising silicon nitride and directly contacting said channel region; and

a gate electrode contacting said gate insulator;

wherein said channel region is interposed between the gate insulator and another insulator.

10. A thin film transistor comprising:

a non-single crystalline semiconductor layer doped with a hydrogen or halogen and having an intrinsic conductivity type and having a channel region disposed in the semiconductor layer;

source and drain regions [in contact with] forming respective junctions with said channel region where the channel region is disposed between said source and drain regions whereby charge carriers move through said channel region between said source and drain regions in a path substantially parallel to said substrate,

a gate insulating film comprising silicon nitride and directly contacting said channel region; and

a gate electrode contacting said gate insulating film;

wherein at least a portion of said channel region contains oxygen in an amount not exceeding $5x10^{18}$ atoms/cm^3;

wherein said channel region is interposed between the gate insulating film and another insulator.

11. A thin film transistor comprising:

a non-single crystalline semiconductor layer doped with a hydrogen or halogen and having an intrinsic conductivity type and having a channel region disposed in the semiconductor layer;

source and drain regions [in contact with] forming respective junctions with said channel region where the channel region is disposed between said source and drain regions whereby charge carriers move through said channel region between said source and drain regions in a path substantially parallel to said substrate,

a gate insulating film comprising silicon nitride and directly contacting said channel region; and

a gate electrode contacting said gate insulating film;

wherein at least a portion of said channel region contains nitrogen in an amount not exceeding $5x10^{18}$ atoms/cm^3;

wherein said channel region is interposed between the gate insulating film and another insulator.

12. A thin film transistor comprising:

a non-single crystalline semiconductor layer doped with a hydrogen or halogen and having an intrinsic conductivity type and having a channel region disposed in the semiconductor layer;

source and drain regions [in contact with] forming respective junctions with said channel region where the channel region is disposed between said source and drain regions whereby charge carriers move through said channel region between said source and drain regions in a path substantially parallel to said substrate,

a gate insulating film comprising silicon nitride and directly contacting said channel region; and

a gate electrode contacting said gate insulating film;

wherein at least a portion of said channel region contains carbon in an amount not exceeding $5x10^{18}$ atoms/cm^3;

wherein said channel region is interposed between the gate insulating film and another insulator.

94. Newly added Claims 13-17 recited the following limitations:

13. An insulated-gate field effect transistor comprising:

a non-single crystalline semiconductor layer of an intrinsic conductivity type containing hydrogen or a halogen, said semiconductor layer being disposed over a substrate;

a channel region formed in said semiconductor layer, wherein a concentration of at least one oxygen, carbon, and nitrogen contained in at least one portion of said semiconductor layer is not higher than $5x10^{18}$ atoms/cm^3;

source and drain regions forming respective junctions with said channel region whereby charge carriers move through said channel region between said source and drain regions in a path substantially parallel to said substrate;

a gate insulator contacting said channel region and comprising silicon and nitrogen; and

a gate electrode contacting said gate insulator.

14. An insulated-gate field effect transistor comprising:

a non-single crystalline semiconductor layer of an intrinsic conductivity type containing hydrogen or a halogen, said semiconductor layer being disposed over a substrate;

a channel region formed in said semiconductor layer, wherein a concentration of at least one of oxygen, carbon and nitrogen contained in at least a portion of said channel region is not higher than $5x10^{18}$ atoms/cm^3;

source and drain regions forming respective junctions with said channel region whereby charge carriers move through said channel region between said source and drain regions in a path substantially parallel to said substrate;

a gate insulator contacting said channel region and comprising silicon and nitrogen; and

a gate electrode contacting said gate insulator.

15. A thin film transistor comprising:

a non-single crystalline semiconductor layer containing hydrogen or a halogen and having an intrinsic conductivity type, said semiconductor layer being disposed over a substrate including a channel region disposed in the semiconductor layer;

source and drain region forming respective junctions with said channel region where the channel region is disposed between said source and drain regions whereby charge carriers move through said channel region between said source and drain regions in a path substantially parallel to said substrate,

a gate insulating film contacting said channel region and comprising silicon and nitrogen; and

a gate electrode contacting said gate insulating film;

wherein at least a portion of said channel region contains oxygen in an amount of not exceeding $5x10^{18}$ atoms/cm^3.

16. A thin film transistor comprising:

a non-single crystalline semiconductor layer containing hydrogen or a halogen and having an intrinsic conductivity type, said

semiconductor layer being disposed over a substrate including a channel region disposed in the semiconductor layer;

source and drain region forming respective junctions with said channel region where the channel region is disposed between said source and drain regions whereby charge carriers move through said channel region between said source and drain regions in a path substantially parallel to said substrate,

a gate insulating film contacting said channel region and comprising silicon and nitrogen; and

a gate electrode contacting said insulating film;

wherein at least a portion of said channel region contains nitrogen in an amount of not exceeding $5x10^{18}$ atoms/cm^3.

17. A thin film transistor comprising:

a non-single crystalline semiconductor layer containing hydrogen or a halogen and having an intrinsic conductivity type, said semiconductor layer being disposed over a substrate including a channel region disposed in the semiconductor layer;

source and drain region forming respective junctions with said channel region where the channel region is disposed between said source and drain regions whereby charge carriers move through said channel region between said source and drain regions in a path substantially parallel to said substrate,

a gate insulating film contacting said channel region; and

a gate electrode contacting said gate insulating film and comprising silicon and nitrogen;

wherein at least a portion of said channel region contains carbon in an amount of not exceeding $5x10^{18}$ atoms/cm^3.

6. Notice of Allowability Dated 1/5/96

95. On January 5, 1996, the Examiner issued a Notice of Allowability in response to SEL's Preliminary Amendment filed June 7, 1995 and the Examiner's interview with SEL's representative on September 28, 1995, allowing Claims 8-17 along with drawings filed on

June 7, 1995. In the Notice of Allowability, the Examiner indicated that the oath or declaration was deficient and a substitute oath or declaration was required.

7. Notice of Informal Application Dated 1/5/96

96. On January 5, 1996, the Examiner issued a Notice of Informal Application indicating that the '953 Application did not conform to the rules governing applications because the abstract was not incompliance with 37 C.F.R. 1.72(b). The Examiner further noted that the drawings submitted on June 7, 1995 were not objected to.

8. Notice of Allowance And Issue Fee Due Dated 1/5/96

97. On January 5, 1996, the USPTO issued a Notice of Allowance and Issue Fee Due, stating that the '953 Application had been examined and was allowed for issuance as a patent and that the prosecution on the merits of the '953 Application was closed. The '953 ultimately issued as the '636 Patent on August 6, 1996.

9. Submission of Issue Fee Payment, Supplemental Declaration, Abstract of Disclosure, and Verified English Translations of Japanese Priority Documents Dated 2/2/96

98. On February 2, 1996, SEL filed a Submission of Issue Fee Payment, Supplemental Declaration, Abstract of Disclosure, and Verified English Translations of Japanese Priority Documents. Verified English translations were provided and requested to be made of record and entered into the file of the '953 Application for the following Japanese Priority Application Nos. 59-100250, 59-100251, and 59-100252. Additionally, SEL filed a declaration and power of attorney and the issue fee transmittal.

10. Request for Certificate of Correction Dated 9/27/96

99. On September 27, 1996, SEL filed a Request for Certificate of Correction identifying errors that SEL stated were of a "clerical or typographical nature," in Claim 10 of the '636 Patent, as well as the correct name of the patentee of U.S. Patent No. 4,578,304 ("the '304

Patent"). In Claim 10, SEL indicated that the phrase "and comprising silicon and nitrogen" was inserted by the typist after the recitation "a gate electrode contacting said gate insulating film" rather than after the preceding recitation "a gate insulating film contacting said channel region" and that this error could "clearly be seen from a comparison of claim 10 with claim 6-9 of the patent." SEL argued that issuance of the Certificate of Correction for this error would not require reexamination of the patent because revised Claim 10 is consistent with Claims 6-9 of the patent, and "inasmuch as the scope of claim 7, for example, is broader than that of corrected claim 10."

100. SEL further sought correction of Claims 1-5 of the '636 Patent, explaining that the antecedent basis was "inadvertently not provided for the term 'substrate' occurring in the phrase 'whereby charge carriers move through said channel region between said source and drain regions in a path substantially parallel to said substrate.'" SEL argued that the issuance of the Certificate of Correction for this error would not require reexamination of the patent stating "present claims 6-10 already recite the antecedent basis for the term 'substrate,' these claims, of course, having also already been examined."

11. Request for Second Certificate of Correction Dated 1/20/97

101. On January 20, 1997, SEL filed a Request for Second Certificate of Correction, noting that an error of a clerical or typographical nature was discovered in corrected Claim 2, wherein the words "one oxygen, carbon and nitrogen contained in at least" which were present in Claim 2 of the published patent were inadvertently omitted in the Certificate of Correction.

12. Notice Re: Certificates of Correction Dated 3/26/97

102. On March 26, 1997, the USPTO requested a response to certain questions regarding the Request for Certificate of Correction, including whether the "change(s) requested under 37 C.F.R. 1.323 constitute new matter or require reexamination of the application" and

whether the "change(s) requested under 37 C.F.R. 1.323 materially affect the scope or meaning of the claims allowed by the examiner in the patent." Notes by the Examiner on the Certificate of Correction dated June 30, 1997, indicate that the "[a]nswer to both questions should be no and the corrections requested should be allowed."

13. Certificate of Correction Dated 8/12/97

103. On August 12, 1997, the USPTO issued a Certificate of Correction, correcting the errors identified by SEL in its first and second Requests for Certificate of Correction, including in Claims 2, 6-10, and the name of the patentee for the '304 Patent.

14. Notice Re: Certificates of Correction Dated 3/4/98

104. On March 4, 1998, the USPTO responded to SEL's Request for Certificate of Correction regarding the '636 Patent. The USPTO requested a response to certain questions regarding the request for certificate of correction, including: (1) whether the "change(s) requested under 37 C.F.R. 1.323 constitute new matter or require reexamination of the application;" (2) whether the "change(s) requested under 37 C.F.R. 1.323 materially affect the scope or meaning of the claims allowed by the examiner in the patent;" and (3) whether the "patent should be read as shown in the certificate of correction." Notes by the Examiner on the Certificate of Correction indicated that the answers to the first two questions was "no" and the third was "yes."

VI. THE '463 PATENT

A. Claim of Priority

105. On June 30, 1980, SEL filed Japanese Patent Application 55-88974 ("the '974 Japanese Application"), which was published as Japanese Unexamined Patent Application Publication S57-13777 on January 23, 1982. The '974 Japanese Application named as inventors Dr. Yamazaki and Mr. Yujiro Nagata. The '463 Patent claims priority to the '974 Japanese

Application, and I understand that SEL contends that the asserted claims of the '463 Patent are entitled to the priority of the '974 Japanese Application. *See* SEL's Responses to Defendants' First Set of Interrogatories at p. 5. I also understand that the issue of whether the claims of the '463 Patent are entitled to claim priority to the '974 Japanese Application is a contested issue.

106. On February 24, 1981, SEL filed U.S. Patent Application No. 06/237,609 ("the '609 Application"), which issued as U.S. Patent No. 4,409,134. On June 29, 1981, SEL filed U.S. Patent Application No. 06/278,418 ("the '418 Application"), which is a continuation-in-part of the '609 Application and which issued as U.S. Patent No. 4,581,620. On September 13, 1985, SEL filed U.S. Patent Application No. 06/775,767 ("the '767 Application"), which is a divisional of the '418 Application and which is now abandoned. On September 18, 1987, SEL filed U.S. Patent Application No. 07/098,705 ("the '705 Application"), which is a continuation of the '767 Application and which is now abandoned. On March 5, 1990, SEL filed U.S. Patent Application No. 07/488,102 ("the '102 Application"), which is a divisional of the '705 Application and which issued as U.S. Patent No. 5,091,334. On October 23, 1990, SEL filed U.S. Patent Application No. 07/601,437 ("the '437 Application"), which is a continuation of the '102 Application and which is now abandoned. I understand that SEL contends that the asserted claims of the '463 Patent are entitled to the priority of the '418, '767, '705, '102, and '437 Applications, but not the '609 Application.[47]

107. The application that eventually matured into the '463 Patent was filed September 8, 1992. This application, U.S. Patent Application No. 08/104,264 ("the '264 Application"), was entitled "Semiconductor Device" and issued on May 31, 2005.[48] The named inventors are identified as Dr. Yamazaki and Dr. Nagata.

[47] *See* SEL's Responses to Defendants' First Set of Interrogatories at p. 5.
[48] *See* the '463 Patent family tree, attached hereto as **Exhibit 4**.

B. Prosecution History of the '636 Patent

1. Originally-Filed Claims

108. The originally-filed patent application contained one independent claim and nine dependent claims. Exemplary Claim 1 recited the following limitations:

> 1. A semiconductor device comprising:
>
> a substrate; and
>
> a non-single crystal semiconductor layer is composed of a first semiconductor region formed primarily of non-single crystal semiconductor and a second semiconductor region formed primarily of a semi-amorphous semiconductor.

2. Preliminary Amendment Dated 10/23/90

109. On October 23, 1990, SEL filed a Preliminary Amendment in which it cancelled Claim 1 and substituted new Claims 11-15. Claim 11 was an independent claim and Claims 12-15 were dependent claims. Exemplary Claim 11 recited the following limitations:

> 11. A semiconductor material comprising a microcrystalline semiconductor selected from group of Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), Si_xGe_{1-x} ($0<x<1$) and the mixture thereof, wherein said microcrystalline semiconductor has lattice strain, the particle size of said microcrystalline is 5-200 A and said semiconductor material is doped with a dangling bond neutralizer selected from the group of hydrogen, chlorine, fluorine and the mixture thereof.

3. Preliminary Amendment Dated 12/20/90

110. On December 21, 1990, SEL filed a Preliminary Amendment in which it cancelled Claims 11-15 and substituted new Claims 16-30. Claims 16, 22, and 29 were independent claims and Claims 17-21, 23-28, and 30 were dependent claims. Exemplary Claims 16, 22, and 29 recited the following limitations:

> 16. A semiconductor material comprising a semiconductor selected from group of Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), Si_xGe_{1-x} ($0<x<1$) and the mixture thereof, wherein said semiconductor is a mixture of crystalline and non-crystalline

> structures of the semiconductor and has lattice strain, said semiconductor material is doped with a dangling bond neutralizer selected from the group of hydrogen, chlorine, fluorine and the mixture thereof at less than 5 mol%.
>
> 22. A semiconductor material comprising a semiconductor selected from group of Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), Si_xGe_{1-x} ($0<x<1$) and the mixture thereof, wherein said semiconductor is a mixture of crystalline and non-crystalline structures of the semiconductor and has lattice strain, said semiconductor material is substantially intrinsic conductivity type and doped with a dangling bond neutralizer selected from the group of hydrogen, chlorine, fluorine and the mixture thereof.
>
> 29. A semiconductor material comprising a semiconductor selected from group of Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), Si_xGe_{1-x} ($0<x<1$) and the mixture thereof, wherein said semiconductor is a mixture of crystalline and non-crystalline structures of the semiconductor and is substantially intrinsic conductivity type, said semiconductor material is doped with a dangling bond neutralizer selected from the group of hydrogen, chlorine, fluorine and the mixture thereof, and diffusion length of minority carriers in said semiconductor material is in the range of 1 to 50 μm.

4. Office Action Dated 2/7/91

111. On February 7, 1991, the USPTO issued an Office Action rejecting Claims 16-30 under 35 U.S.C. § 102(e) as being anticipated in light of U.S. Patent No. 4,239,554 ("the '554 Patent").

5. Examiner Interview Dated 4/9/91

112. On April 9, 1991, Mr. Ferguson, Dr. Yamazaki, Mr. Yanai, and Ms. Nakano attended an interview with the examiner, Mr. Jerome Jackson. The interview record indicates that the attendees discussed certain prior art as well as semi-amorphous material. The notes indicate: "Applicant will submit new references Yamazaki 4,409,134 and Matsuda et al and may change the status of the instant application to a continuation in part of 4,409,134. Discussion of 'semi-amorphous' material."

6. Amendment Dated 5/2/91

113. On May 2, 1991, SEL submitted an Amendment in which it amended its claim of priority with the following statement: "This application is a continuation-in-part of U.S. Application No. 237,607 filed February 24, 1981 (now U.S. Patent No. 4,409,134 issued October 11, 1983)." SEL also amended Claims 16, 22, and 29, and added new Claim 31, which was a dependent Claim. Exemplary Claims 16, 22, and 29 recited the following limitations:

> 16. (Amended) A semiconductor material comprising a semiconductor [selected from group of] comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$) [and the mixture thereof], wherein said semiconductor is in a stable state intermediate the amorphous state and the single crystal state of the semiconductor [a mixture of crystalline and non-crystalline structures of the semiconductor] and has lattice strain[,] and said semiconductor material is doped with a dangling bond neutralizer [selected from the group of] comprising hydrogen[, chlorine,] or fluorine [and the mixture thereof] at less than 5 mol%.
>
> 22. (Amended) A semiconductor material comprising a semiconductor [selected from group of] comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$) [and the mixture thereof], wherein said semiconductor is [a mixture of] crystalline [and non-crystalline structures of the semiconductor] and has lattice strain, where said semiconductor material is substantially intrinsic conductivity type and doped with a dangling bond neutralizer comprising [selected from the group of] hydrogen[, chlorine,] or fluorine [and the mixture thereof] and where the carrier length range of at least the minority carriers in the semiconductor material is at least one micron.
>
> 29. (Amended) A semiconductor material comprising a semiconductor [selected from group of] comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$) [and the mixture thereof], wherein said semiconductor is [a mixture of] crystalline [and non-crystalline] and is substantially intrinsic conductivity type and has lattice strain, where said semiconductor material is doped with a dangling bond neutralizer selected from the group of hydrogen[, chlorine], or fluorine [and the mixture thereof], [and diffusion length of minority carriers in said semiconductor material is in the range of 1 to 50 μm] and wherein said semiconductor material is formed on a substrate having an insulating surface wherein said insulating surface comprises a

material selected from the group consisting of glass, ceramic, and silicon wafer having an insulating surface.

114. In the remarks, SEL stated that "[r]eferring to the rejections of claims 16-30 under 35 U.S.C. 102(e) as being anticipated by Yamazaki '554, the subject application has been made a continuation-in-part of U.S. Patent 4,409,134 ('134)" and was entitled to a filing date of June 29, 1981. SEL also noted the "common subject letter (semi-amorphous semiconductor material) of the claims of the subject application and the '134 patent" entitled the application to the February 24, 1981 filing date of the '134 patent for priority. SEL further explained that certain references were not prior art over the application. For example, SEL explained that the article *Electrical and Structural Properties of Phosphorous-Doped Glow-Discharge Si:F:H and Si:H Films* by Matsuda et al., Japanese Journal of Applied Physics, Vol. 19, No. 6, June 1980, was not available as a reference to the claims of the patent application because the article was directed to photovoltaic devices and thus is not pertinent to the claims.

7. Supplemental Response Dated 5/28/91

115. On May 28, 1991, SEL filed a Supplemental Response to the Amendment filed May 2, 1991, submitting verified English translations of Japanese Application Nos. 53-83467, 53-83468, 53-86867, 53-86868, and 0263880.

8. Information Disclosure Statement Dated 5/30/91

116. On May 30, 1991, SEL filed an Information Disclosure Statement, disclosing Japanese Publications 55-11330, 55-13939, and 55-11329, and attaching English translations of the Japanese Publications.

9. Office Action Dated 8/13/91

117. On August 13, 1991, the USPTO issued an Office Action indicating that Claims 16-31 were rejected under 35 U.S.C. §§ 102(e), 103 and 112 and "under the judicially created

doctrine of obviousness-type double patenting as being unpatentable over claims 1-13 of U.S. Patent No. 4,581,620" because the claims are directed to the same semiconductor material and devices and thus are not patentably distinct. The USPTO also indicated that Claims 1-15 were cancelled. In the comments, the USPTO also stated that there was no publication date for the 026388 Japanese reference and thus it would not be made of record, SEL had not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. § 120, and that the specification was objected to under 35 U.S.C. § 112 as the specification as originally filed does not provide support for the invention as now claimed.

10. Preliminary Amendment Dated 10/30/91

118. On October 30, 1991, SEL filed a Preliminary Amendment in response to the Office Action of August 13, 1991, amending the specification of the subject application. In the remarks, SEL urged that the subject application could properly be made a continuation-in-part of Serial No. 237,609 filed February 24, 1981 (now the '134 Patent).

11. Examiner Interview Dated 11/7/91

119. On November 7, 1991, Mr. Ferguson and Dr. Yamazaki attended an interview with the examiner, Mr. Jackson. The interview record indicates that the attendees discussed continuation-in-part procedures with respect to the '134 Patent, as well as a "discussion of claims with respect to Carbon and Ovshinsky in terms of 'lattice strain' and atomic structure of materials." The interview record also indicates that crystallographic data should be submitted.

12. Amendment Dated 12/11/91

120. On December 11, 1991, SEL filed an Amendment in response to the Office Action of August 13, 1991. The Amendment amended independent Claims 16, 22 and 29 as follows:

16. (Twice Amended) A semiconductor material comprising a

semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$), wherein said semiconductor is [in a stable state intermediate the amorphous state and the single crystal state of the semiconductor] a mixture of microcrystalline and non-crystalline structures of the semiconductor and has a lattice strain and said semiconductor material is doped with a dangling bond neutralizer comprising hydrogen or fluorine [at less than 5 mol%].

22. (Twice Amended) A semiconductor material comprising a semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$) [and the mixture thereof], wherein said semiconductor is a mixture of [crystalline] microcrystalline and non-crystalline structures of the semiconductor and has lattice strain, where said semiconductor material is substantially intrinsic conductivity type and doped with a dangling bond neutralizer comprising hydrogen or fluorine and where the carrier length range of at least the minority carriers in the semiconductor material is at least one micron.

29. (Twice Amended) A semiconductor material comprising a semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$), wherein said semiconductor is a mixture of microcrystalline [crystalline] and non-crystalline structures of the semiconductor and is substantially intrinsic conductivity type and has lattice strain, where said semiconductor material is doped with a dangling bond neutralizer selected from the group of hydrogen or fluorine and wherein said semiconductor material is formed on a substrate having an insulating surface wherein said insulating surface comprises a material selected from the group consisting of glass, ceramic, and silicon wafer having an insulating surface.

121. In the remarks, SEL stated that Japanese Application No. 026388 ("the '388 Japanese Application") is the priority application upon which the '134 Patent is based on is not a reference with respect to the subject application. SEL also stated that although it disagreed with the examiner regarding whether the conditions for receiving the benefit under 35 U.S.C. § 120 had been complied with, it was submitting amendments of intervening abandoned applications Serial Nos. 775,767, filed September 13, 1985, and 98,705 filed September 18, 1987. SEL also

noted a reissue application of U.S. Patent 4,581,620 ("the '620 Patent") would be filed shortly in accordance with the requirements of the August 13, 1991 Office Action.

122. SEL further noted in the remarks that the specification is now in accord with 35 U.S.C. § 112 with the amendment of claims 16, 22, and 29. SEL also urged that the '554 Patent by Yamazaki was no longer prior art over Claims 16-31, and that SEL would be filing a Terminal Disclaimer with respect to the '620 Patent. SEL also remarked that Claims 16-28 and 31, as amended, distinguish over U.S. Patent No. 4,485,389 ("Ovshinsky"), and that rejection of Claims 29 and 30 over Ovshinsky in view of U.S. Patent No. 3,151,379 ("Escoffery") was overcome as Escoffery does not cure the deficiencies of Ovshinsky. Finally, SEL stated that rejection of Claims 16-31 over Yamazaki '938 or '939 in view of Ovshinsky was also overcome because the '938 and '939 Patents fail to cure the deficiencies of Ovshinsky.

13. Notice of Filing Reissue Application Dated 2/7/92

123. On February 7, 1992, SEL filed a Notice of Reissue Application in the subject application of U.S. Patent No. 4,581,620 ("the '620 Patent"), and submitted the reissue application of the '620 Patent.

14. Office Action Dated 3/5/92

124. On March 5, 1992, the USPTO issued an Office Action rejecting Claims 16-31 under 35 U.S.C. § 102(e) as being anticipated by, or in the alternative, under 35 U.S.C. § 103 as obvious in light of Yamazaki '554, and rejecting Claims 16-28 and 31 under 35 U.S.C. § 102(e) as being anticipated by, or in the alternative, under 35 U.S.C. § 103 as obvious in light of Ovshinsky '389. Additionally, the USPTO provisionally rejected Claims 16-31 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-13 of "copending application Serial No. 4,581,620." The USPTO further rejected Claims 29 and 30 under 35 U.S.C. § 103 as being unpatentable over Ovshinsky in view of

Escoffery, and rejected Claims 16-30 under 35 U.S.C. § 103 as being unpatentable over Yamazaki '938 or '939 in view of Ovshinsky. The USPTO further explained that a "string of codependency has to be met to U.S. 06/237,609 for applicant to claim benefits under 35 USC 120, and further the application must contain or be amended to contain a specific reference to the earlier filed application." Finally, the USPTO noted that the Office Action is made final.

15. Examiner Interview Dated 7/29/92

125. On July 29, 1991, Mr. Ferguson and Dr. Yamazaki attended an interview with the examiner, Mr. Jackson. The interview record indicates that the applicant "proposes eliminating fluorine from the claim structure and adding hydrogen at less than 5 mol %. Applicant also proposes submitting evidence distinguishing claims over the '938 and '939 references by showing a difference in lattice strain or other structure." The notes further indicate that the "changes proposed are after final and may not be entered."

16. Request For File Wrapper Continuing Application Under 37 C.F.R. 1.62 Dated 9/8/92

126. On September 8, 1992, the USPTO received a Request for File Wrapper Continuing Application Under 37 C.F.R. 1.62. The Request for File Wrapper Continuing Application was by named inventors Dr. Yamazaki and Dr. Nagata. In the submission, the specification was also amended to state:

> This application is a continuation of Serial No. 07/601,437, filed October 23, 1990, now abandoned, which itself was a continuation of Serial No. 07/488,705, filed September 18, 1987, which was a continuation of Serial No. 06/775,767, filed September 13, 1985, abandoned, which was a divisional of Serial No. 06/278,418, filed June 29, 1981, now U.S. Patent No. 4,581,620.

127. Additionally, SEL claimed priority under 35 U.S.C. § 119 based on Japanese Application No. 88974/80.

17. Request For File Wrapper Continuing Application Under 37 C.F.R. 1.62 Dated 9/11/92

128. On September 11, 1992, the USPTO received a Request for File Wrapper Continuing Application under 37 C.F.R. 1.62. The Request for File Wrapper Continuing Application was by named inventors Dr. Yamazaki and Dr. Nagata. In the submission, the specification was also amended to state:

> This application is a continuation of Serial No. 07/601,437, filed October 23, 1990, now abandoned, which itself was a continuation of Serial No. 07/488,705, filed September 18, 1987, which was a continuation of Serial No. 06/775,767, filed September 13, 1985, abandoned, which was a divisional of Serial No. 06/278,418, filed June 29, 1981, now U.S. Patent No. 4,581,620.

129. Additionally, SEL claimed priority under 35 U.S.C. § 119 based on Japanese Application No. 88974/80.

18. Request For File Wrapper Continuing Application Under 37 C.F.R. 1.62 Dated 10/21/92

130. On October 21, 1992, the USPTO received a Request for File Wrapper Continuing Application under 37 C.F.R. 1.62. The Request for File Wrapper Continuing Application was by named inventors Dr. Yamazaki and Dr. Nagata. In the submission, the specification was also amended to state:

> This application is a continuation of Serial No. 07/601,437, filed October 23, 1990, now abandoned, which itself was a continuation of Serial No. 07/488,705, filed September 18, 1987, which was a continuation of Serial No. 06/775,767, filed September 13, 1985, abandoned, which was a divisional of Serial No. 06/278,418, filed June 29, 1981, now U.S. Patent No. 4,581,620.

131. Additionally, SEL claimed priority under 35 U.S.C. § 119 based on Japanese Application No. 88974/80.

19. Preliminary Amendment and Rule 132 Declaration Dated 12/11/92

132. On December 11, 1992, SEL filed a Rule 132 Declaration and Preliminary Amendment to amend independent Claims 16-29 and add new independent Claims 32-34. SEL amended Claims 16-29 as follows:

> 16. (Three Times Amended) A semiconductor material comprising a semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$), wherein said semiconductor is N type of P type and is a mixture of [micro]crystalline and non-crystalline structures of the semiconductor and has a lattice strain and said semiconductor material is doped with a dangling bond neutralizer comprising hydrogen [or fluorine] at less than 5 mol % and excluding fluorine.
>
> 22. (Three Times Amended) A semiconductor material comprising a semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$) wherein said semiconductor is a mixture of [micro]crystalline and non-crystalline structures of the semiconductor and has lattice strain, where said semiconductor material is substantially intrinsic conductivity type and doped with a dangling bond neutralizer comprising hydrogen [or fluorine] at less than five mol % and excluding fluorine and where the [carrier] diffusion length range of at least the minority carriers in the semiconductor material is at least one micron.
>
> 29. (Three Times Amended) A semiconductor material comprising a semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$), wherein said semiconductor is a mixture of [micro]crystalline and non-crystalline structures of the semiconductor and is substantially intrinsic conductivity type and has lattice strain, where said semiconductor material is doped with a dangling bond neutralizer comprising [selected from the group of] hydrogen [or fluorine] at less than five mol % and excluding fluorine, and wherein said semiconductor material is formed on a substrate having an insulating surface wherein said insulating surface comprises a material selected from the group consisting of glass, ceramic, and silicon wafer having an insulating surface.

133. New independent Claims 32-34 recited the following limitations:

> 32. A semiconductor material comprising a semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$),

> or Si_xGe_{1-x} ($0<x<1$), wherein said semiconductor is N type or P type and is a mixture of crystalline and non-crystalline structures of the semiconductor and has a lattice strain and said semiconductor is doped with a dangling bond neutralizer consisting essentially of hydrogen at less than five mol %.
>
> 33. A semiconductor material comprising a semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$), wherein said semiconductor is a mixture of crystalline and non-crystalline structures of the semiconductor and has a lattice strain, where said semiconductor material is substantially intrinsic conductivity type and doped with a dangling bond neutralizer consisting essentially of hydrogen at less than five mol % and where the diffusion length range of at least the minority carriers in the semiconductor material is at least one micron.
>
> 34. A semiconductor material comprising a semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$), wherein said semiconductor is a mixture of crystalline and non-crystalline structures of the semiconductor and is substantially intrinsic conductivity type and has lattice strain where said semiconductor material is doped with a dangling bond neutralizer consisting essentially of hydrogen at less than five mol %, and wherein said semiconductor material is formed on a substrate having an insulating surface wherein said insulating surface comprises a material selected from the group consisting of glass, ceramic, and silicon wafer having an insulating surface.

134. In the Remarks, SEL stated that it had filed an application for the reissue of the '620 Patent. SEL further stated that all prior rejections had been overcome.

135. SEL also filed the Executed Rule 132 Declaration of Dr. Yamazaki, one of the named inventors and applicants of the '437 Patent Application. The Declaration recited experiments conducted under Dr. Yamazaki's supervision "demonstrating the existence of a semi-amorphous state (SAS) in accordance with the present invention, which state exists between the amorphous and crystalline states."

20. Declaration Under 37 CFR 1.132 Dated 12/11/92

136. On December 11, 1992, SEL filed a Declaration of Dr. Yamazaki detailing experiments conducted under Dr. Yamazaki's supervision that SEL claimed demonstrated the existence of a semi-amorphous state in accordance wit the subject invention.

21. Supplemental Filing of Executed Rule 132 Declaration Dated 1/25/93

137. On January 25, 1993, SEL filed a Supplemental Filing of Executed Rule 132 Declaration of Dr. Yamazaki.

22. Supplemental To the Preliminary Amendment and Rule 132 Declaration Dated 9/8/93

138. On September 8, 1993, SEL filed a Supplement to the Preliminary Amendment and Rule 132 Declaration that SEL had filed on December 11, 1992. In the remarks, SEL stated that the claims of the '264 Patent Application had overcome the prior rejections.

23. Office Action Dated 10/15/93

139. On October 15, 1993, the USPTO issued an Office Action rejecting Claims 16-34. The USPTO indicated that Claims 16-28 and 31-33 were rejected under 35 U.S.C. § 102(e) as anticipated by, or in the alternative, under 35 U.S.C. § 103 as obvious over Ovshinsky. The USPTO further stated that the previous rejection still applied, and that the new limitation of "excluding fluorine" did not distinguish over Ovshinsky because Ovshinsky claims amorphous alloy material with hydrogen dangling bond neutralizer and excluding fluorine. The USPTO further stated that Claims 29, 30 and 34 were rejected under 35 U.S.C. § 103 as being unpatentable over Ovshinsky in view of Escoffery, and that Claims 16-21 and 32 were rejected under 35 U.S.C. § 102(b) as anticipated by, or in the alternative, under 35 U.S.C. § 103 as obvious over Matsuda. The USPTO also stated that Claims 16-34 were rejected under 35 U.S.C.

§ 103 as being unpatentable over Yamazaki ‘939 or ‘938. Finally, the USPTO stated that the declaration filed by SEL was insufficient to overcome the rejection of Claims 16-34.

24. Amendment Dated 2/14/94

140. On February 14, 1994, SEL filed an Amendment, amending independent Claims 16, 22, 29, and 32-34, and adding new dependent Claims 35-40. Exemplary Claims 16, 22, 29, and 32-34 recited the following limitations:

> 16. (Four Times Amended) A semiconductor material <u>for a semiconductor device</u> comprising a semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$), wherein said semiconductor is N type of P type and is a mixture of [micro]crystalline and non-crystalline structures of the semiconductor and has a lattice strain and said semiconductor material is doped with a dangling bond neutralizer comprising hydrogen at less than 5 mol % and excluding fluorine.
>
> 22. (Four Times Amended) A semiconductor material <u>for a semiconductor device</u> comprising a semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$) wherein said semiconductor is a mixture of [micro]crystalline and non-crystalline structures of the semiconductor and has lattice strain, where said semiconductor material is substantially intrinsic conductivity type and doped with a dangling bond neutralizer comprising hydrogen at less than five mol % and excluding fluorine and where the diffusion length range of at least the minority carriers in the semiconductor material is at least one micron.
>
> 29. (Four Times Amended) A semiconductor material <u>for a semiconductor device</u> comprising a semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$), wherein said semiconductor is a mixture of [micro]crystalline and non-crystalline structures of the semiconductor and is substantially intrinsic conductivity type and has lattice strain, where said semiconductor material is doped with a dangling bond neutralizer comprising hydrogen at less than five mol % and excluding fluorine, and wherein said semiconductor material is formed on a substrate having an insulating surface wherein said insulating surface comprises a material selected from the group consisting of glass, ceramic, and silicon wafer having an insulating surface.

32. (Amended) A semiconductor material <u>for a semiconductor device</u> comprising a semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$), wherein said semiconductor is N type or P type and is a mixture of crystalline and non-crystalline structures of the semiconductor and has a lattice strain and said semiconductor is doped with a dangling bond neutralizer consisting essentially of hydrogen at less than five mol %.

33. (Amended) A semiconductor material <u>for a semiconductor device</u> comprising a semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$), wherein said semiconductor is a mixture of crystalline and non-crystalline structures of the semiconductor and has a lattice strain [, where] <u>and wherein a particular size of crystals contained in said semiconductor material is within a range of 5-200Å</u> [said semiconductor material is substantially intrinsic conductivity type and doped with a dangling bond neutralizer consisting essentially of hydrogen at less than five mol % and where the diffusion length range of at least the minority carriers in the semiconductor material is at least one micron].

34. (Amended) A semiconductor material <u>for a semiconductor device</u> comprising a semiconductor comprising Si, Ge, Si_3N_{4-x} ($0<x<4$), SiO_{2-x} ($0<x<2$), SiC_x ($0<x<1$), or Si_xGe_{1-x} ($0<x<1$), wherein said semiconductor is a mixture of crystalline and non-crystalline structures of the semiconductor and is substantially intrinsic conductivity type and has lattice strain where said semiconductor material is doped with a dangling bond neutralizer consisting essentially of hydrogen at less than five mol %, and wherein said semiconductor material is formed on a substrate having an insulating surface wherein said insulating surface comprises a material selected from the group consisting of glass, ceramic, and silicon wafer having an insulating surface.

141. In the remarks, SEL stated that the claims of the ‘264 Patent Application had overcome the prior rejections.

25. Office Action Dated 5/9/94

142. On May 9, 1994, the USPTO issued an Office Action rejecting Claims 16-40. Specifically, the USPTO rejected Claims 16-28, 31-33, 35-36, and 38-39 under 35 U.S.C. § 102(e) as anticipated by, or in the alternative, under 35 U.S.C. § 103 as obvious over

Ovshinsky. The USPTO further rejected Claims 29-30, 34, 347 and 40 under 35 U.S.C. § 103 as being unpatentable over Ovshinsky in view of Escoffery. Additionally, the USPTO rejected Claims 16-21, 32, 35, and 38 under 35 U.S.C. § 102(b) as anticipated by, or in the alternative, under 35 U.S.C. § 103 as obvious over Matsuda. Finally, the USPTO rejected Claims 16-40 under 35 U.S.C. § 103 as being unpatentable over Yamazaki '939 or '938 in view of Ovshinsky, and under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-3 of the '134 Patent.

26. Amendment Dated 11/9/94

143. On November 9, 1994, SEL filed an Amendment, amending the specification and cancelling Claims 22-28, 31, 33, and 26. The specification was amended to state as follows:

> This application is a continuation of Serial No. 07/601,437 filed October 23, 1990, now abandoned, which itself was a continuation of Serial No. 07/488,102, filed March 5, 1990 (now U.S. Patent No. 5,091,334), which was a divisional of Serial No. 07/098,705 filed September 18, 1987, which was a continuation of Serial No. 06/775,767 filed September 13, 1985, abandoned, which was a divisional of Serial No. 06/278,418 filed June 29, 1981 (now U.S. Patent No. 4,581,620), which was a continuation-in-part of Serial No. 237,609 (now U.S. Patent No. 4,409,134).

144. In the remarks, SEL stated that the claims of the '264 Application had overcome the prior rejections.

27. Amendment of Abandoned Application Dated 11/9/94

145. On November 9, 1994, SEL filed an Amendment of Abandoned Application, amending the specification for the abandoned subject application in order to establish a chain of copendency under 35 U.S.C. § 120 between pending U.S. Application No. 08/104,264 filed September 8, 1992 and Application Serial No. 237,609 (now the '134 Patent). The specification was amended as follows:

> This application is a continuation of Serial No. 07/488,102, filed

March 5, 1990 (now U.S. Patent No. 5,091,334), which was a divisional of Serial No. 07/098,705 filed September 18, 1987, which was a continuation of Serial No. 06/775,767 filed September 13, 1985, abandoned, which was a divisional of Serial No. 06/278,418 filed June 29, 1981 (now U.S. Patent No. 4,581,620), which was a continuation-in-part of Serial No. 237,609 (now U.S. Patent No. 4,409,134).

28. Office Action Dated 6/2/95

146. On June 2, 1995, the USPTO issued an Office Action rejecting Claims 16-21, 29, 30, 32, 34-35, 37-38, and 40. Specifically, the USPTO rejected Claims 16-21, 32, 35 and 38 under 35 U.S.C. § 102(e) as anticipated by, or in the alternative, under 35 U.S.C. § 103 as obvious over Ovshinsky. The USPTO also rejected Claims 29-30, 34, 37 and 40 under 35 U.S.C. § 103 as being unpatentable over Ovshinsky in view of Escoffery. The USPTO rejected Claims 16-21, 29, 30, 32, 34-35, 37-38, and 40 under 35 U.S.C. § 103 as being unpatentable over Yamazaki '939 or '938 in view of Ovshinsky, and under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-3 of the '134 Patent. The USPTO also noted that the Office Action was made final.

29. Request For File Wrapper Continuing Application Under 37 CFR 1.62 and For Corrected Filing Receipt Dated 11/16/95

147. On November 16, 1995, the USPTO received a Request For File Wrapper Continuing Application Under 37 C.F.R. § 1.62 and for Corrected Filing Receipt. In the Request For File Wrapper Continuing Application Under 37 C.F.R. § 1.62, SEL indicated that the request was for filing a continuation of the prior pending application Serial No. 07/601,437 ("the '437 Patent Application") by Dr. Yamazaki and Dr. Nagata. The Request also amended the specification by indicating it was a continuation of the '437 Patent Application, and indicated that priority was claimed under 35 U.S.C. § 119 based on Japanese Application No. 88974/80.

148. Additionally, in the Request for Corrected Filing Receipt, SEL stated that the filing receipt states the incorrect filing date and application number.

30. Notice of Appeal and Amendment Dated 12/4/95

149. On December 4, 1995, SEL filed a Notice of Appeal of the Patent Board of Appeals decision of June 2, 1995 rejecting Claims 16-21, 29-30, 32, 34-35, 37-38 and 40, and an Amendment. In the Amendment, SEL sought to cancel Claims 16-21, 29-30, 32, 34-35, 37-38 and 40 without prejudice, and add new Claims 41-59. New Claims 41, 47 and 53 were independent claims and new Claims 42-46, 48-52, and 54-59 were dependent claims. Exemplary Claims 41, 47 and 53 recited the following limitations:

> 41. A semiconductor material for a semiconductor device consisting essentially of (a) a semiconductor selected from the group consisting of silicon, germanium and a combination thereof, (b) hydrogen, and (c) a metal element wherein said semiconductor material has a crystalline structure.
>
> 47. A semiconductor material for a semiconductor device comprising (a) a semiconductor selected from the group consisting of silicon, germanium, and a combination thereof, (b) a recombination center neutralizer containing hydrogen and excluding fluorine, and (c) a metal element wherein said semiconductor material has a crystalline structure and a concentration of said recombination center neutralizer is not higher than 5 mol %.
>
> 53. A semiconductor material for a semiconductor device comprising (a) a semiconductor selected from the group consisting of silicon, germanium and a combination thereof, (b) a recombination center neutralizer containing hydrogen and excluding fluorine, and (c) a metal element wherein said semiconductor material has a crystalline structure and a concentration of said metal element is not higher than 10 mol %.

150. In the remarks, SEL stated that the claims of the ‘264 Patent Application, as amended, had overcome the prior rejections. SEL also noted that the claims of the ‘264 Patent Application were related to those of copending application Serial No. 08/470,559.

31. Advisory Action Dated 12/20/95

151. On December 20, 1995, the USPTO issued an Advisory Action. In the Advisory Action, the USPTO indicated that the Appellant's brief was due, that the Appellant's response to the final rejected filed December 4, 1995 (noted as December 6, 1995) had been considered, but was not deemed to place the application in condition for allowance. The USPTO indicated that the proposed amendments to the claims and/or specification would not be entered and the final rejection stood because: (a) there was no convincing showing under 37 C.F.R. 1.116(b) why the proposed amendment was necessary and not earlier presented, (b) the new limitation "a metal element" raised new issues that would require further consideration and/or search, and (c) they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal.

152. The USPTO also indicated that upon the filing of an appeal, the proposed amendment would not be entered and claims 16-21, 29-30, 32, 34-35, 37-38 and 40 would be rejected.

32. Request Under 37 C.F.R. 1.129 To Withdraw Finality Of Final Rejection Dated 1/17/96

153. On January 17, 1996, SEL filed a Request Under 37 C.F.R. 1.129 to Withdraw Finality of the Final Rejection of June 2, 1995, and that the December 4, 1995 amendment be considered on the merits.

33. Office Action Dated 1/29/96

154. On January 29, 1996, the USPTO issued an Office Action provisionally rejecting Claims 41-59 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 45-104 of copending application Serial No. 08/470,559. The USPTO stated that although the claims were not identical, "they are not patentably distinct from each

other because the semiconductor material of '264 is claimed in '599." The USPTO further stated that Claims 45, 51 and 57 were rejected under 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The USPTO also rejected Claims 42, 48, and 54 under 35 U.S.C. § 112 for lack of enablement and failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The USPTO rejected Claims 41, 43-44, 46-47, 49-50, 52-54, 55-56 and 58-59 under 35 U.S.C. § 103 as being unpatentable over Ovshinsky in view of Yamazaki '938 or '939.

155. The USPTO noted that Claims 45, 51 and 57 would be allowable if rewritten to overcome the rejection under 35 U.S.C. § 112 and to include all of the limitations of the base claim and any intervening claims.

34. Amendment Dated 4/29/96

156. On April 29, 1996, SEL filed an Amendment, amending Claims 41, 45, 47, 51, 53 and 57. Claims 41, 47, and 53 were independent claims, and Claims 45 and 51 were dependent claims. Exemplary Claims 41, 47, and 53 recited the following limitations:

> 41. (Amended) A semiconductor material for a semiconductor device consisting essentially of (a) a semiconductor selected from the group consisting of silicon, germanium and a combination thereof, (b) hydrogen, and (c) a metal element wherein said semiconductor material has a <u>non-single</u> crystalline structure.
>
> 47. (Amended) A semiconductor material for a semiconductor device comprising (a) a semiconductor selected from the group consisting of silicon, germanium, and a combination thereof, (b) a recombination center neutralizer containing hydrogen and excluding fluorine, and (c) a metal element wherein said semiconductor material has a <u>non-single</u> crystalline structure and a concentration of said recombination center neutralizer is not higher than 5 mol %.
>
> 53. (Amended) A semiconductor material for a semiconductor device comprising (a) a semiconductor selected from the group

> consisting of silicon, germanium and a combination thereof, (b) a recombination center neutralizer containing hydrogen and excluding fluorine, and (c) a metal element wherein said semiconductor material has a non-single crystalline structure and a concentration of said metal element is not higher than 10 mol %.

157. In the remarks, SEL stated that the claims, as amended, had overcome the prior art rejections.

35. Office Action Dated 7/11/96

158. On July 11, 1996, the USPTO issued an Office Action rejecting Claims 41-59. Specifically, the USPTO rejected Claims 42, 48, and 54 under 35 U.S.C. § 112 for lack of enablement, and/or for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The USPTO provisionally rejected Claims 41-59 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 45-104 of copending application Serial No. 08/470,559 on the ground that the claims were not patentably distinct from each other because the semiconductor material of '264 is claimed in '559. The USPTO rejected Claims 41, 43-44, 46-47, 49-50, 52-53, 55-56, and 58-59 under 35 U.S.C. § 103 as being unpatentable over Ovshinsky in view of Yamazaki '938 or '939. Claims 45, 51, and 57 were also objected to as being dependent upon a rejected base claim, but the USPTO stated that they would be allowed if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Finally, the USPTO stated that the arguments filed by the appellant on May 1, 1996 were considered but were not deemed persuasive because "phosphorous, P, is a well-known n-type dopant, and antimony, Sb, can also function as an n-type dopant." Additionally, the "applicant's arguments regarding 'metal element' are unconvincing of patentability" and the "new recitation in the claims 'non-single crystal' does not structurally distinguish over the applied art which likewise teaches non-single crystal materials."

36. Amendment And Request Under 37 CFR 1.129 To Withdraw Finality Of Final Rejection Dated 10/11/96

159. On October 11, 1996, SEL filed an Amendment and Request Under 37 C.F.R. 1.129 to Withdraw Finality of the Final Rejection. In the Amendment, SEL cancelled Claims 22-28, 31, 36, 39 and 41-59, and added new Claims 60-80. Claims 60, 67, 70, and 78 were independent claims, and Claims 61-66, 68-69, 71-77, and 79-80 were dependent claims. Exemplary Claims 60, 67, 70, and 78 were as follows:

> 60. A non-single crystalline semiconductor material having at least one junction between two semiconducting regions of differing electrical properties, said semiconductor material comprising silicon and doped with dangling bond neutralizer comprising hydrogen or a halogen, wherein said non-single crystalline semiconductor material is interposed between a first amorphous insulating surface and a second amorphous insulating nitride.
>
> 67. A non-single crystalline semiconductor material having at least one junction between two semiconducting regions of differing electrical properties, said semiconductor material comprising silicon and doped with dangling bond neutralizer comprising hydrogen or a halogen, wherein a portion of said junction is in direct contact with an amorphous insulating nitride.
>
> 70. A non-single crystalline semiconductor material comprising silicon and having a mixture of crystalline and amorphous structures supported by an amorphous insulating surface, said semiconductor material doped with dangling bond neutralizer comprising hydrogen or a halogen at less than 5 mol % and having lattice strain.
>
> 78. A non-single crystalline semiconductor material comprising silicon and having a crystalline structure supported by an amorphous insulating surface, said semiconductor material doped with dangling bond neutralizer comprising hydrogen or a halogen at less than 5 mol % and having lattice strain.

160. In the remarks, SEL stated that new independent Claim 60 "is directed to a non-single crystalline semiconductor material having a junction and is characterized in that the semiconductor material is interposed between a first amorphous insulating surface and a second

amorphous insulating nitride." SEL also stated that new independent Claim 67 "is similar to Claim 60 but is different in that a portion of the junction is in direct contact with an amorphous insulating nitride." SEL stated that these claims "may be relevant to the subject matter of the copending application Serial No. 08/371,486."

37. Information Disclosure Statement Dated 11/25/96

161. On November 25, 1996, SEL filed an Information Disclosure Statement, stating that certain references were cited in related application Serial Nos. 08/371,486 and 07/928,181. The references included, for example: *National Convention Record, the Institute of Electronics and Communication Engineers of Japan*, 2-285 - 2-288, Matsumura et al., (March 1980) (including partial translation); and P.G. LeComber, et. al., *Amorphous-Silicon Field-Effect Device and Possible Applications* (Mar. 15, 1976).

38. Office Action Dated 1/8/97

162. On January 8, 1997, the USPTO issued an Office Action rejecting Claims 60-80 under 35 U.S.C. § 103(a) as being "unpatentable over Matsumura March 1980 'a-Si FET IC integrated on a glass substrate' in view of Yamazaki Jp 55-111330, LeComber March 1979, and Ovshinsky '941." The USPTO explained that Matsumura "teaches a thin film fet comprising an amorphous insulating glass substrate, an intrinsic amorphous silicon channel layer with junctions to n-type amorphous silicon source and drain regions, and a silicon dioxide gate insulating layer." The USPTO further explained that from Yamazaki it would have been "obvious to have included hydrogen or halogen dangling bond neutralizers in Matsumura, or to have practice semi-amorphous silicon material with short range order 'crystalline structure' with lattice strain for the a-silicon semiconductor material of Matsumura to improve the device performance." Additionally, "[f]rom LeComber it would have been obvious to have practiced or substituted a

silicon nitride gate insulator for the silicon dioxide gate insulator of Matsumura because LeComber shows the nitride to be an effective gate insulator for thin film fet devices."

39. Information Disclosure Statement Dated 7/8/97

163. On July 8, 1997, SEL filed a Petition for Extension of Time requesting a three month extension and Information Disclosure Statement. In the Information Disclosure Statement, SEL provided copies of certain foreign references and an explanation of the relevance of the references not in English.

40. Amendment Dated 7/8/97

164. On July 8, 1997, SEL filed an Amendment in which it cancelled Claims 60-80 without prejudice or disclaimer to the subject matter and added new Claims 81-95. Claims 81, 85 and 88 were independent claims and Claims 82-84, 86-87 and 89-95 were dependent claims. Exemplary Claims 81, 85 and 88 were as follows:

> 81. A thin film transistor comprising:
>
> a pair of source and drain regions;
>
> a channel region between said source and drain regions; and
>
> a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween,
>
> said channel region comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;
>
> said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and having an impurity conductivity type to form junctions in contact with said channel region,
>
> wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprises a nitride.

85. A thin film transistor comprising:

a pair of source and drain regions;

a channel region between said source and drain regions; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween,

said channel region comprising an intrinsic non-single semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;

said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and having a P or N type conductivity to form PI or NI junctions in contact with said channel region,

wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprise a nitride.

88. A thin film transistor comprising:

a non-single crystalline semiconductor film having at least source, drain and channel regions;

a gate insulating film adjacent to said channel region; and

a gate electrode adjacent to said channel region with said gate insulating film therebetween,

wherein said non-single crystalline semiconductor film contains a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and at least a portion of said gate insulating film which is in contact with said channel region comprises a nitride.

165. In the remarks, SEL directed the examiner's attention to copending application Serial No. 08/371,486, which SEL stated was directed to similar subject matter as the current pending claims. SEL also stated that "LeComber establishes that LeComber uses a silicon nitride gate insulating layer in his particular device, which has Schottky junctions that do <u>not</u>

contact the silicon nitride layer. In particular, LeComber simply states that a glass substrate which carries a series of thin evaporated A1 strips is covered with a film of silicon nitride by a glow discharge technique. There is no further statement by LeComber with respect to the silicon nitride layer, its functions, or its advantages and thus it is improper for the examiner to conclude, as done in that application, that LeComber 'clearly suggests a SiN gate insulating layer for other thin film transistors…' in addition to the particular transistor employed in the LeComber test." SEL also stated that in the related '486 application, LeComber is the only reference disclosing a silicon nitride film, and that the type of transistor disclosed by LeComber is different from that disclosed by Weitzel and Matsumura because the LeComber transistor utilizes a Schottky or semiconductor-oxide-metal junction.

41. Supplemental Information Disclosure Statement And Interview Summary Dated 7/18/97

166. On July 18, 1997, the USPTO received a Supplemental Information Disclosure Statement and Interview Summary filed by SEL. In the filing, SEL stated that a telephone conference occurred on July 9, 1997 with SEL's representative, Mr. Robinson and the Examiner, Mr. Jackson. The Interview Summary states that during the call, the parties discussed SEL's Information Disclosure Statement filed on November 25, 1996, as well as the fact that "several references on the 1449 returned to Applicant with the Official Action mailed January 8, 1997 were lined through." The notes indicate that the Examiner stated that this may have occurred if the references were duplicates of references previously submitted or if copies were not included with the Information Disclosure Statement. SEL included additional copies of the references.

42. Submission of Declaration Under 37 CFR 1.132 Dated 7/18/97

167. On July 18, 1997, the USPTO received a Submission of Declaration Under 37 C.F.R. 1.132 filed by SEL. The Declaration was executed by Dr. Yamazaki and detailed his

education and work background experience, and detailed experiments conducted under Dr. Yamazaki's direction in response to the Office Action of November 22, 1996, in order to demonstrate the "unexpected advantages associated with the claimed invention."

43. Office Action Dated 10/20/97

168. On October 20, 1997, the USPTO issued an Office Action rejecting Claims 81-95 under 35 U.S.C. § 103(a) as being "unpatentable over Matsumura 3/80 in view of Yamazaki Jp '330, LeComber 3/79, Ovshinsky '941, and further in view of Madan (J. of Non-Crystalline Solids) 1976." The USPTO stated that "there is clear suggestion in the prior art for practicing thin film amorphous field effect transistor devices with silicon nitride gate insulating material. LeComber and Madan show devices with nitride insulator and Madan particularly discloses advantages. It is prima facie obvious to practice silicon nitride gate insulation in thin film amorphous field effect transistors."

44. Examiner Interview Dated 4/23/98

169. On April 23, 1998, Mr. Robinson and Dr. Yamazaki attended an interview with the examiner, Mr. Jackson. The interview record indicates that the attendees discussed the LeComber, Madan and Matsumura prior art references. The notes indicate: "Applicants emphasize the superiority of SiN gate insulator material for thin film structure including hydrogenated source and drain regions."

45. Amendment Dated 4/28/98

170. On April 28, 1998, SEL filed an Amendment, cancelling Claims 94-95, amending Claims 81, 84, 85, 87-88 and 91-93, and adding new Claims 96-98. Claims 81, 85, 88 and 96-98 were independent Claims, and Claims 87 and 91-93 were dependent claims. Exemplary Claims 81, 85 and 86 were as follows:

81. (Amended) A thin film transistor comprising:

a pair of source and drain regions;

a channel region between said source and drain regions; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween,

said channel region comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;

said pair of source and drain regions comprising [a non-single crystal] an amorphous silicon semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and having an impurity conductivity type to form junctions in contact with said channel region,

wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprises a nitride; and

wherein at least a portion of said junctions are covered by another insulator different from said gate insulator.

85. (Amended) A thin film transistor comprising:

a pair of source and drain regions;

a channel region between said source and drain regions; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween,

said channel region comprising an intrinsic [non-single] amorphous silicon semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;

said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and having a P or N type conductivity to form PI or NI junctions in contact with said channel region,

wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprise a nitride; and

wherein at least a portion of said junctions are covered by another insulator different from said gate insulator.

88. (Amended) A thin film transistor comprising:

a [non-single crystalline] semiconductor film having at least source, drain and channel regions comprising amorphous silicon, said source and drain regions forming junctions with said channel region;

a gate insulating film adjacent to said channel region; and

a gate electrode adjacent to said channel region with said gate insulating film therebetween,

wherein said [non-single crystalline] amorphous silicon semiconductor film contains a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and at least a portion of said gate insulating film which is in contact with said channel region comprises a nitride; and

wherein at least a portion of said junctions are covered by another insulator different from said gate insulator.

171. New Claims 96-98 recited the following limitations:

96. A thin film transistor comprising:

a pair of source and drain regions;

a channel region between said source and drain regions; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

said channel region comprising an amorphous silicon semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;

said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and

a combination thereof, and having an impurity conductivity type to form junctions in contact with said channel region,

wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprises a nitride;

wherein said channel region is interposed between said gate insulator and another insulator different from said gate insulating film; and

wherein at least a portion of said junctions are covered by said another insulator.

97. A thin film transistor comprising:

a pair of source and drain regions;

a channel region between said source and drain regions; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween,

said channel region comprising an intrinsic amorphous silicon semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;

said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and having a P or N type conductivity to form PI or NI junctions in contact with said channel region,

wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprises a nitride; and

wherein said channel region is interposed between said gate insulator and another insulator different from said gate insulating film; and

wherein at least a portion of said junctions are covered by said another insulator.

98. A thin film transistor comprising:

a semiconductor film having at least source, drain and channel

> regions comprising amorphous silicon, said source and drain regions forming junctions with said channel region;
>
> a gate insulating film adjacent to said channel region; and
>
> a gate electrode adjacent to said channel region with said gate insulating film therebetween;
>
> wherein said amorphous silicon semiconductor film contains a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and at least a portion of said gate insulating film which is in contact with said channel region comprises a nitride; and
>
> wherein said channel region is interposed between said gate insulator and another insulator different from said gate insulating film; and
>
> wherein at least a portion of said junctions are covered by an insulator.

172. In the remarks, SEL stated that the pending claims had been amended to further distinguish them from the prior art, including LeComber and Madan, and that the "amendments together with the superior results achieved thereby are sufficient in view of the controlling precedent to overcome any case of *prima facie* obviousness." SEL also stated that "at least a portion of the junctions between the source and drain regions and the channel region are covered by another insulator different from the gate insulator" and that "this further distinguishes the present invention from the combination of Matsumura, LeComber and Madan." Finally, SEL stated that "the devices relied upon to reject the present invention (LeComber and Madan) are '<u>of a completely different type</u>'…. That is, both of LeComber and Madan disclose devices having Schottky junctions that do not contact the gate insulating layer, while the present invention, as claimed, is limited to a device having junctions between the source and drain regions and the channel region."

46. Information Disclosure Statement Dated 4/28/98

173. On April 28, 1998, SEL filed an Information Disclosure Statement, requesting that certain references be made of record in the '264 Application, and attaching copies of the references.

47. Information Disclosure Statement Dated 5/6/98

174. On May 6, 1998, SEL filed an Information Disclosure Statement, requesting that certain references be made of record in the '264 Application, and attaching copies of the references, including an English translation of the article M. Matsumura, et al., *A-Si FET IC Integrated on a Glass Substrate* (Mar. 1980).

48. Notice of Abandonment Dated 10/9/98

175. On October 9, 1998, the USPTO issued a Notice of Abandonment in view of the applicant's failure to timely file a proper response to the Office Action dated October 20, 1997.

49. Response to Notice of Abandonment Dated 10/27/98

176. On October 27, 1998, the USPTO received a Response to Notice of Abandonment filed by SEL. SEL stated that the Notice of Abandonment was issued in error.

50. Response Dated 10/27/98

177. On October 27, 1998, the USPTO received a Response to its January 8, 1997 Office Action filed by SEL. In the Response, SEL stated that the claimed invention was advantageous, and that with regard to the LeComber reference relied upon by the examiner, "LeComber uses a silicon nitride gate insulating layer in his particular device, which has Schottky junctions that do not contact the silicon nitride layer…LeComber simply states that a glass substrate which carries a series of thin evaporated A1 strips is covered with a film of silicon nitride by a glow discharge technique. There is no further statement by LeComber with respect to the silicon nitride layer, its functions, or its advantages."

51. Office Action Dated 1/14/99

178. On January 14, 1999, the USPTO issued an Office Action rejecting Claims 81-93, and 96-98 under 35 U.S.C. § 103(a) as being "unpatentable over Matsumura 3/80 in view of Yamazaki '330, LeComber 3/79, Ovshinsky '941, Madan 1976 and further in view of Yamazaki '663." The USPTO stated that the advantages SEL argues are not taught be LeComber or Madan are "not taught in the original disclosure but are asserted in a declaration. The prior art teaches and suggests nitride insulator for thin film transistors…" The USPTO further stated that "[t]he nitride in the prior art had been used as gate insulating materials in both Matsumura and Madan" and that the arguments "regarding the 'another' insulation layer are unpersuasive because it would have been obvious from '663 to form an overcoat layer in a device as Matsumura, etc., as a final passivation layer or for planarization etc. as taught in '663." The USPTO also noted that the action was made final.

52. Response Dated 1/20/99

179. On January 20, 1999, SEL filed a Response to the Examiner's Official Action dated January 8, 1997. In its Response, SEL stated that the "claimed structure of the present invention is particularly advantageous" because "when junctions (such as source/channel and drain/channel junctions) are formed between non-single crystalline semiconductor materials doped with hydrogen or a halogen, bonds between silicon and hydrogen or a halogen near these junctions…are broken…resulting in a degradation in device characteristics." SEL stated that the claimed invention solves this problem. SEL further stated that LeComber "uses a silicon nitride gate insulating layer…which has Schottky junctions that do not contact the silicon nitride layer." Thus, LeComber does not disclose a device where "junctions (such as source/drain and drain/channel junctions) are formed between non-single crystalline semiconductor materials."

53. Information Disclosure Statement Dated 7/13/99

180. On July 13, 1999, SEL filed an Information Disclosure Statement requesting that certain references be made of record in the application, and attaching copies of the references.

54. Notice of Appeal Dated 7/14/99

181. On July 14, 1999, SEL filed a Notice of Appeal to the Board of Appeals from the decision dated January 14, 1999 as to all rejected claims, including Claims 81-93 and 96-98. In the Appeal, SEL states that "it appears that Matsumura is relied upon for the teaching of a thin film FET including an undoped or intrinsic channel region and n+ doped source and drain regions" and "LeComber is said to suggest practicing or substituting a silicon nitride gate insulator for the silicon dioxide gate insulator of Matsumura." SEL also stated that "the Examiner simply states it would be obvious to use the silicon nitride layer of LeComber or Madan in that device without providing a sufficient showing that one of ordinary skill in the art would have been motivated to do so especially at the time the invention of the subject application was made."

182. With regard to LeComber, SEL stated that "LeComber uses a silicon nitride insulating layer in his particular device, which has Schottky junctions" and that "[t]here is no further statement by LeComber with respect to the silicon nitride layer, its functions, or its advantages. Absent any teaching of the advantages of silicon nitride or any problems from the use of silicon oxide, it is respectfully submitted that one of skill in the art would not, without more, have been motivated to combine LeComber with the other references." SEL also stated that "if both SiN and SiO insulating layers were obvious in view of the cited references at the time of the invention, as asserted, it would appear that ample references teaching a SiN insulating layer in a device as presently claimed would be available and it would not be necessary to attempt to find a suggestion in either LeComber or Madan to use a SiN gate

insulating layer in Matsumura's device. However, no such references have been presented." Finally, SEL further stated that LeComber, Madan and Matsumura do not disclose or suggest "'another insulator' or any desirability therefore" and that "the limitation that at least a portion of the junctions between the source and drain regions and the channel region are covered by another insulator" further distinguishes the present invention from the combination of Matsumura, LeComber and Madan.

55. Examiner Interview Dated 7/20/99

183. On July 29, 1999, Mr. Robinson and Mr. Eisen attended an interview with the examiner, Mr. Jackson. The interview record indicates that: "Applicants argue that Powell '85 and '89 show superior TFT performance with silicon nitride gate insulation. Limitations in independent claims regarding 'another insulator' will be deleted by amendment."

56. After Final Amendment Dated 9/21/99

184. On September 21, 1999, SEL filed an After Final Amendment cancelling Claims 91 and 93 without prejudice or disclaimer and amending independent Claims 81, 85, 88 and 96-98. Claims 81, 85, 88 and 96-98 were amended as follows:

> 81. (Twice Amended) A thin film transistor comprising:
>
> a pair of source and drain regions;
>
> a channel region between said source and drain regions; and
>
> a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween,
>
> said channel region comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;
>
> said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and

a combination thereof, and having an impurity conductivity type to form junctions in contact with said channel region,

wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprises a nitride[; and

wherein at least a portion of said junctions are covered by another insulator different from said gate insulator].

85. (Twice Amended) A thin film transistor comprising:

a pair of source and drain regions;

a channel region between said source and drain regions; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween,

said channel region comprising an intrinsic amorphous silicon semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;

said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and having a P or N type conductivity to form PI or NI junctions in contact with said channel region,

wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprise a nitride[; and

wherein at least a portion of said junctions are covered by another insulator different from said gate insulator].

88. (Twice Amended) A thin film transistor comprising:

a semiconductor film having at least source, drain and channel regions comprising amorphous silicon, said source and drain regions forming junctions with said channel region;

a gate insulating film adjacent to said channel region; and

a gate electrode adjacent to said channel region with said gate insulating film therebetween,

wherein said amorphous silicon semiconductor film contains a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and at least a portion of said gate insulating film which is in contact with said channel region comprises a nitride[; and

wherein at least a portion of said junctions are covered by another insulator different from said gate insulator].

96. (Amended) A thin film transistor comprising:

a pair of source and drain regions;

a channel region between said source and drain regions; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

said channel region comprising an amorphous silicon semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;

said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and having an impurity conductivity type to form junctions in contact with said channel region,

wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprises a nitride;

wherein said channel region is interposed between said gate [insulator] insulating film and another insulator different from said gate insulating film; and

wherein at least a portion of said junctions are covered by said another insulator.

97. (Amended) A thin film transistor comprising:

a pair of source and drain regions;

a channel region between said source and drain regions; and

a gate electrode adjacent to said channel region with a gate

insulating film interposed therebetween,

said channel region comprising an intrinsic amorphous silicon semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;

said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and having a P or N type conductivity to form PI or NI junctions in contact with said channel region,

wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprises a nitride; and

wherein said channel region is interposed between said gate [insulator] <u>insulating film</u> and another insulator different from said gate insulating film; and

wherein at least a portion of said junctions are covered by said another insulator.

98. (Amended) A thin film transistor comprising:

a semiconductor film having at least source, drain and channel regions comprising amorphous silicon, said source and drain regions forming junctions with said channel region;

a gate insulating film adjacent to said channel region; and

a gate electrode adjacent to said channel region with said gate insulating film therebetween;

wherein said amorphous silicon semiconductor film contains a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and at least a portion of said gate insulating film which is in contact with said channel region comprises a nitride; and

wherein said channel region is interposed between said gate [insulator] <u>insulating film</u> and another insulator different from said gate insulating film; and

wherein at least a portion of said junctions are covered by [an] <u>said another</u> insulator.

185. In the remarks, SEL noted that the pending claims had been amended, consistent with the examiner interview on July 20, 1999, to limit the number of issues to decide on appeal.

57. Examiner's Answer Dated 12/10/99

186. On December 10, 1999, the USPTO issued an Examiner's Answer in response to SEL's appeal brief. In the Answer, the USPTO stated that "the elements [of the claimed structure] were fundamental in the art of thin film transistors and clearly their practice together would not appear to be unusual or unexpected to one of ordinary skill. Both silicon oxide and silicon nitride gate insulating films in field effect transistor devices were well known at the time of applicant's invention and there is clearly a preponderance of evidence that their practice in thin film transistor devices was not and would not have been unobvious. There are no unexpected results in appellant's practice of silicon nitride gate insulating films. The prior art applied expects the nitrides films to be advantages." The USPTO concluded that the rejections should be sustained.

58. Reply Brief and Request For Oral Hearing Dated 2/1/00

187. On February 1, 2000, SEL filed a Reply Brief and Request for Oral Hearing regarding the appeal. In the Reply Brief, SEL stated that it was the USPTO's burden to show a motivation to combine the references cited by the USPTO as invalidating prior art, and that the superiority of silicon nitride as a gate insulator would not have been expected.

59. Information Disclosure Statement and Notice of Litigation Under MPEP 2001.06(C) Dated 12/23/02

188. On December 23, 2003, SEL filed an Information Disclosure Statement and Notice of Litigation directing the USPTO's attention to the ongoing litigation between SEL and Acer Incorporated, Acer America Corporation, and AU Optronics Corporation (the "Acer

Litigation"), including the inequitable conduct contentions included in Acer's affirmative defenses, and enclosing copies of certain pleadings from the litigation.

60. Order Remanding To Examiner Dated 12/31/02

189. On December 31, 2002, the Board of Patent Appeals and Interferences issued an Order Remanding to the Examiner the application for: (1) consideration of the Information Disclosure Statement dated November 25, 1996; (2) appropriate notification by the examiner to appellants of such consideration; (3) status on entry or non-entry of the amendment filed May 6, 1998; (4) disposition of Claim 94; and (5) for such further action as may be appropriate.

61. Office Communication Dated 2/6/03

190. On February 6, 2003, the USPTO issued an Office Communication stating that Claim 94 was cancelled by amendment on May 6, 1998.

62. Information Disclosure Statement and Notice of Litigation Under MPEP 2001.06(C) Dated 3/3/03

191. On March 3, 2003, SEL filed an Information Disclosure Statement and Notice of Litigation disclosing the Acer Litigation and attaching pleadings from the same, including Acer's invalidity contentions and additional references.

63. Order Vacating Oral Hearing and Order Remanding To Examiner Dated 4/21/03

192. On April 21, 2003, the Board of Patent Appeals and Interferences issued an Order Vacating the Oral Hearing and Order Remanding the application to the examiner to consider the Information Disclosure Statement and Notice of Litigation filed by SEL and for further action as may be appropriate.

64. Information Disclosure Statement and Notice of Litigation Under MPEP 2001.06(C) Dated 4/28/03

193. On April 28, 2003, SEL filed an Information Disclosure Statement and Notice of Litigation regarding the Acer Litigation, stating that Acer had filed an amended complaint and that SEL had asserted claims for infringement of one or more U.S. Patents 6,355,941, 6,404,480, 6,404,476 and 5,929,527, and that U.S. Patent No. 6,355,941 was in the same family as the subject application.

65. Office Communication Dated 5/21/03

194. On May 21, 2003, the USPTO issued an Office Communication indicating the examiner had considered the Information Disclosure Statement and Notice of Litigation filed by SEL.

66. Office Communication Dated 8/26/03

195. On August 26, 2003, the USPTO issued an Office Communication indicating that the application had been returned to the Board of Appeals for consideration.

67. Information Disclosure Statement and Notice of Litigation Under MPEP 2001.06(C) Dated 9/22/03

196. On September 22, 2003, the USPTO received an Information Disclosure Statement and Notice of Litigation filed by SEL regarding the Acer Litigation, submitting the Final Claim Construction Order and Final Invalidity Contentions from the Acer Litigation.

68. Information Disclosure Statement and Notice of Litigation Under MPEP 2001.06(C) Dated 10/8/03

197. On October 8, 2003, SEL filed an Information Disclosure Statement and Notice of Litigation regarding the Acer Litigation, stating that the litigation had been dismissed as the result of a stipulated dismissal between the parties, and submitting certain pleadings from the

litigation, including the Motions for Summary Judgment filed by the parties and accompanying declarations and Supplemented Final Invalidity Contentions filed by Acer.

69. Order Remanding to Examiner Dated 10/15/03

198. On October 15, 2003, the Board of Patent Appeals and Interferences remanded the application to the examiner to consider the Information Disclosure Statements filed August 22, September 4, September 11, and September 15, 2003.

70. Office Communication Dated 10/22/03

199. On October 22, 2003, the USPTO issued an Office Communication stating that it had considered the Information Disclosure Statements filed on August 22, September 4, September 11, and September 15, 2003 and was forwarding the application to the Board of Appeals for consideration.

71. Order Remanding to Examiner Dated 11/6/03

200. On November 6, 2003, the Board of Patent Appeals and Interferences remanded the application to the examiner to consider the Information Disclosure Statements filed on April 30 and October 8, 2003.

72. Office Communication Dated 12/4/03

201. On December 4, 2003, the USPTO issued an Office Communication stating that it had considered the Information Disclosure Statements filed on April 30 and October 8, 2003.

73. Information Disclosure Statement Dated 2/16/04

202. On February 16, 2004, SEL filed an Information Disclosure Statement disclosing certain patents that had come to SEL's attention, including U.S. Patent No. 4,390,791 ("the '791 Patent") which SEL stated that a third party claimed invalidated Claims 3, 6-7, 10-16, 19-21, 23-, 25-, 27-28, 30-33, and 35 of the '941 Patent. SEL also attached pages from the '791 Patent.

74. Office Communication Dated 4/27/04

203. On April 27, 2004, the USPTO issued an Office Communication stating that it had considered the Information Disclosure Statement filed on April 20, 2004.

75. Decision On Appeal Dated 5/27/04

204. On May 27, 2004, the Board of Patent Appeals and Interferences issued its decision reversing the examiner's final rejection of claims 81-90, 92 and 96-98. The Board of Patent Appeals stated its finding that a prima facie case for unpatentability of the claimed subject matter had not been established to sustain the rejection of Claims 81-90, 92 and 96-98 under 35 U.S.C. § 103 as being unpatentable over Matsumura, Yamazaki '330, LeComber, Madan, and Yamazaki '663.

76. Notice of Allowance and Fee(s) Due Dated 6/24/04

205. On June 24, 2004, the USPTO issued a Notice of Allowance and Fee(s) Due in response to the Board of Appeals Decision of May 27, 2004, allowing Claims 81-90, 92, and 96-98, and acknowledging foreign priority for the application.

C. Assignments Related to the '463 Patent

1. Assignment by Joint Inventors Dated 6/25/81

206. On June 25, 1981, Dr. Nagata purportedly executed an Assignment by Joint Inventors agreement, assigning the invention claimed in the United States patent application for the "Semiconductor Device" invention, as claimed in Japanese Patent Application No. 88974/80, to Dr. Yamazaki.[49]

2. Declaration and Power of Attorney Dated 6/25/81

207. On June 25, 1981, Dr. Yamazaki and Dr. Nagata purportedly executed a Declaration and Power of Attorney, appointing Mr. Ferguson as their attorney with full power of

[49] SEL-SAM0038495-50.

substitution and revocation to prosecute the United States patent application for the "Semiconductor Device" invention, as claimed in Japanese Patent Application No. 88974/80, filed June 30, 1980.[50]

3. Assignment Dated 9/25/91 and 9/30/91

208. On September 25 and 30, 1991, Dr. Yamazaki and Dr. Nagata, respectively, purportedly executed an Assignment agreement assigning his interest in the invention claimed in the United States patent application for the "Method For Forming MIS Field Effect Transistors" to SEL.[51]

4. Substitute Declaration and Power of Attorney For Patent Application Dated 9/25/91 and 9/30/91

209. On September 25 and 30, 1991, Dr. Yamazaki and Dr. Nagata, respectively, purportedly executed a Substitute Declaration and Power of Attorney for Patent Application, appointing Mr. Ferguson as their attorney with full power of substitution and revocation to prosecute the United States patent application for the "Method For Forming MIS Field Effect" invention, as claimed in Serial No. 07/488,102, the specification for which was filed on Mach 5, 1990.[52]

5. Assignment of Patent Application or Patent Dated 12/16/91

210. On December 16, 1991, SEL filed the Assignment of Patent Application or Patent, purporting to record an assignment by Dr. Nagata to SEL, dated December 11, 1991, for the invention claimed in U.S. Patent Application No. 07/488,102, filed on March 5, 1990 (now U.S. Patent No. 5,091,334).[53]

[50] SEL-SAM0001363-64.
[51] SEL-SAM0056698-99.
[52] SEL-SAM0056700-701.
[53] SEL-SAM0122934-35.

VII. DISCUSSION

A. Examples of the Breach of the Duty of Candor Related to the '463 Patent

211. I have been asked to formulate an opinion regarding whether Dr. Yamazaki breached his duty of candor and good faith in connection with prosecution of the '463 Patent. The materials I have reviewed in this case make apparent at least the following examples where the duty of candor expected by the USPTO was breached in connection with the '463 Patent. In particular, I believe that the following documents and information would have been highly material to a reasonable examiner in determining the patentability of the '463 Patent: (1) certain materials and information from the action titled *Semiconductor Energy Laboratory Co., Ltd., v. Samsung Electronics Ltd., et al.*, Case No. 96-1460-A ("*SEL I*"); and (2) U.S. Patent No. 4,072,974 ("the '974 Patent"). As explained below, Dr. Yamazaki and his patent attorneys did not advise the examiner regarding certain material information from the *SEL I* litigation or the existence of the '974 Patent during prosecution of the '463 Patent. As also explained below, Dr. Yamazaki's inequitable conduct during the prosecution of the '636 Patent had an immediate and necessary relation to the '463 Patent and provided Dr. Yamazaki an advantage in connection with the '463 Patent.

212. I may supplement the information below upon review of additional materials in this case, such as (for example) any expert reports submitted by SEL, additional deposition testimony, information, documents, pleadings, allegations, rulings, and/or trial testimony and exhibits.

1. Dr. Yamazaki's Concealment of Material Information From the *SEL I* Litigation

213. I understand that in obtaining the '463 Patent, Dr. Yamazaki and his patent attorneys, Mr. Ferguson and Mr. Robinson, failed to inform the USPTO regarding certain

material information arising from litigation between SEL and Samsung involving the '636 Patent. That information included the Motion for Reconsideration and accompanying Matsumura Declaration filed by SEL in an attempt to overturn the district court's finding of inequitable conduct in the *SEL I* litigation.

214. On October 10, 1996, Dr. Yamazaki's company, SEL, instituted an action against Samsung in the Eastern District of Virginia for infringement of the '636 Patent, styled *Semiconductor Energy Laboratory Co., Ltd., v. Samsung Electronics Ltd., et al.,* Case No. 96-1460-A ("*SEL I*"). Samsung filed its Amended Answer and Counterclaims to SEL's First Amended Complaint on September 4, 1997, claiming that the '636 Patent was unenforceable by virtue of SEL's inequitable conduct.

215. On April 15, 1998, following a seven-day bench trial, the district court found that the '636 Patent was unenforceable due to SEL's inequitable conduct during prosecution of the '636 Patent before the USPTO.[54] In so holding, the district court held that SEL had intentionally withheld Japanese Laid-Open Application No. 56-135968 ("the Canon reference") even though SEL had submitted the reference to the USPTO because of the manner in which SEL had submitted the reference.[55] Specifically, by submitting only a partial translation of the Canon reference along with an explanation of the reference that omitted key material teachings of the reference, SEL essentially withheld the reference from the USPTO.[56]

216. The district court also found that SEL had intentionally misrepresented the materiality of a 1983 article by C.C. Tsai, entitled "*Amorphous Si Prepared in a UHV Plasma*

[54] *Semiconductor Energy Laboratory Co., Ltd., v. Samsung Electronics Co., Ltd.,* 4 F. Supp. 2d 477 (E.D. Va. 1998) ("*SEL I*"), *recon. den'd,* 24 F. Supp. 2d 537 (E.D. Val. 1998), *aff'd* 204 F.3d 1368 (Fed. Cir. 2000).
[55] *SEL I,* 4 F. Supp. 2d at 484.
[56] *Id*.

*Deposition Syste*m."[57] In particular, the district court found that SEL mischaracterized the Tsai article as applying primarily to solar cells rather than TFTs, thus intentionally misleading the examiner into believing that the Tsai article was not material.[58]

217. The district court further found that Dr. Yamazaki had "compromised his fundamental duty of candor to the PTO" and intended to deceive the USPTO during the prosecution of the '636 Patent.[59]

218. In an effort to overturn the district court's finding of inequitable conduct, SEL filed a Motion for Reconsideration. In the Motion for Reconsideration, SEL argued that Dr. Yamazaki's failure to disclose a full translation of the Canon reference should not have been considered inequitable conduct because it was cumulative of the article M. Matsumura, et al., *A-Si FET IC Integrated on a Glass Substrate* (Mar. 1980) ("Matsumura") modified in view of other prior art such as the article P.G. LeComber, et. al., *Amorphous-Silicon Field-Effect Device and Possible Applications* (Mar. 15, 1976) ("LeComber").[60] Both the Matsumura reference and LeComber were of record in the '636 Patent Application.

219. SEL argued to the district court that the only relevant difference between the Matsumura reference and the Canon reference was that Matsumura's gate insulator was made of silicon oxide rather than silicon nitride:

> Fig. 1 of Matsumura, like Canon, discloses a coplanar TFT with

[57] *Id.* at 486.
[58] *Id.*
[59] *SEL I*, 4 F. Supp. at 494-96; Notably, the MPEP includes several references to the *SEL I* litigation involving Dr. Yamazaki's inequitable conduct. (*See* MPEP §§ 609, 2004.6, and 2004.7 (Eighth Ed., August 2001)). For example, the *SEL I* litigation is cited by the MPEP in support of advising applicants to take "special care" to see that information is not incorrectly or incompletely characterized. The MPEP had long provided that advice, but now cites the *SEL I* case as an example. (*See e.g.*, MPEP § 2004.7 (Fifth Ed., August 1983)).
[60] Revised Memorandum in Support of Motion of Plaintiff SEL for Reconsideration of Inequitable Conduct Ruling, dated May 1, 1998 ("Mot. for Reconsideration") at 11 (SAMS00878190-8223).

> the same intrinsic amorphous silicon sandwiching structure found in the '636 patent. The only difference in structure is the gate insulator. In Matsumura, the gate insulator is made of silicon oxide rather than silicon nitride.[61]

According to SEL, however, that difference "was suggested by other information before the PTO."[62] SEL stated that "the use of silicon nitride as a gate insulator was spelled out from the Examiner several times, including in connection with the discussion of Matsumura." *Id.* at 12. In particular, SEL stated that the use of silicon nitride as a gate insulator could be supplied by combining the teachings of Matsumura with information from LeComber, which SEL argued was highlighted for the examiner as follows: "[t]he Examiner's attention is particularly directed to Reference (18) to LeComber et al. which appears to disclose the use of a silicon nitride layer as a gate insulating layer."[63]

220. In support of its Motion for Reconsideration, SEL submitted the declaration of Masakiyo Matsumura ("Matsumura Declaration"), the author of the Matsumura prior art reference.[64] The Matsumura Declaration stated that the silicon oxide in the Matsumura reference "can be replaced with silicon nitride as the gate insulator when I consider" LeComber.[65] SEL concluded:

> Thus, having a single reference showing silicon nitride in combination with the intrinsic amorphous silicon sandwiching structure is not material, given that the combination is clearly taught by other information before the PTO. As noted above, this other information informed the Examiner of the prior art use of silicon nitride as a gate insulator and its known interchangeability

[61] *Id.*
[62] *Id*.
[63] *Id.* at 12 (quoting Information Disclosure Statement (November 15, 1995) at 4 ('636 prosecution history)).
[64] Mot. for Reconsideration, Exh. E. (Declaration of Masakiyo Matsumura, dated April 27, 1998 ("Matsumura Decl.") (SAMS00898136-149)).
[65] Matsumura Decl. at ¶ 6.

with silicon oxide.[66]

221. However, before and after the above litigation activity, Dr. Yamazaki took a different position when prosecuting his '463 Patent Application in the USPTO. In the '463 Patent Application, the USPTO had issued a rejection of all claims over Matsumura, LeComber, and two other references. The examiner had stated, *inter alia*:

> From LeComber it would have been obvious to have practiced or substituted a silicon nitride gate insulator for the silicon dioxide gate insulator of Matsumura because LeComber shows the nitride to be an effective gate insulator for thin film fet devices.[67]

222. Dr. Yamazaki opposed that argument of unpatentability by submitting an Amendment of the '463 Patent Application claims and his own declaration. In the Amendment, Dr. Yamazaki disputed the combinability of LeComber and Matsumura and argued that LeComber does *not* suggest a silicon nitride (SiN) gate insulating layer for other thin film transistors:

> LeComber uses a silicon nitride gate insulating layer in his particular device, which has Schottky junctions that do <u>not</u> contact the silicon nitride layer. In particular, LeComber simply states that a glass substrate which carries a series of thin evaporated A1 strips is covered with a film of silicon nitride by a glow discharge technique. There is no further statement by LeComber with respect to the silicon nitride layer, its functions, or its advantages and thus it is improper for the examiner to conclude, as done in that application, that LeComber "clearly suggests a SiN gate insulating layer for <u>other</u> thin film transistors…" in addition to the particular transistor employed in the LeComber test (emphasis added).
>
> * * * * *
>
> With respect to LeComber and the combination relied on in the related '486 application, it is important to note that the type of transistor disclosed by LeComber is entirely different from the transistor by Weitzel and Matsumura. That is, while the transistor

[66] Mot. for Reconsideration at 13.
[67] Office Action (January 8, 1997) at 2 ('463 prosecution history) (SAMS00768743).

> disclosed by Weitzel and Matsumura has junctions between two semiconductor materials having different conductivity types, the transistors of LeComber utilizes a Schottky junction, that is, a semiconductor-oxide-metal jacket.[68]

223. Additionally, Dr. Yamazaki's declaration attempted to show unexpected results from substituting silicon nitride for silicon oxide in a portion of a gate insulating layer in contact with the channel region.[69]

224. Still, the examiner was not convinced, and Dr. Yamazaki filed an appeal to the Board of Patent Appeals and Interferences. In his Appeal Brief, Dr. Yamazaki argued that there was no motivation to combine LeComber with the Matsumura reference,[70] again noting that the type of transistor disclosed by LeComber is "entirely different" than the transistor disclosed in the Matsumura reference.[71]

225. Dr. Yamazaki's arguments were successful. The Board of Appeals noted Dr. Yamazaki's position that LeComber's structure is "entirely different" than Matsumura's,[72] and included the following text in its opinion:

> We agree with appellants that the teaching of LeComber would not have been considered by the artisan as applicable to the type of device disclosed by Matsumura, and thus would not have suggested modification of the device…[T]he references disclose different structures, and LeComber does not discuss the reference's teachings as applied to other environments. Nor has the examiner supplied evidence (i.e., explanatory or supporting references) in support of the assertion, or provided a convincing rationale as to why LeComber, taken with Matsumura, would have rendered obvious the proposed modification.[73]

[68] Amendment (July 10, 1997) at 8 ('463 prosecution history) (SAMS00768864).
[69] Submission of Declaration Under 37 CFR 1.132 at 2 ('463 prosecution history) (SAMS00768743).
[70] Appeal Brief (September 14, 1999) at 8-9 ('463 prosecution history) (SAMS00768953-54).
[71] Appeal Brief at 13 (SAMS00768958).
[72] Decision on Appeal (May 27, 2004) at 4 ('463 prosecution history) (SAMS00769428).
[73] *Id.* at 5 (SAMS00769429).

226. I understand that Samsung's technical expert, Dr. Fair, is of the opinion that the above-described litigation activity was inconsistent with the above-described prosecution position. For example, when urging the court to combine the transistors described in the Matsumura reference with those in LeComber, Dr. Yamazaki contended that one of ordinary skill in the art would have known of the interchangeability of silicon oxide and silicon nitride as a gate insulator.[74] But when arguing *against* their combination to the USPTO, Dr. Yamazaki said that the type of transistor disclosed by LeComber is "entirely different" than the transistor disclosed in the Matsumura reference, and that LeComber does *not* suggest a silicon nitride gate insulating layer for other thin film transistors such as those in the Matsumura reference.[75] Some of the inconsistent statements are in the table below:[76]

Statements in SEL's '463 Patent File History	**Statements in SEL's Motion for Reconsideration and Matsumura Decl.**
"[I]t is improper for the examiner to conclude…that LeComber clearly suggests a SiN gate insulating layer for other thin film transistors." (Amendment at 8, Jul. 8, 1997). "With respect to LeComber and the combination relied on in the related '486 application, it is important to note that the type of transistor disclosed by LeComber is ***entirely different*** from the transistor disclosed in Weitzel and Matsumura. … For all these reasons, . . . it is respectfully submitted that the [sic] a *prima facie* case of obvious cannot be maintained . . . ." (*Id.* at 8-9 (emphasis	"[T]he use of silicon nitride as a gate insulator was spelled out from the Examiner several times, including in connection with the discussion of Matsumura's intrinsic amorphous silicon sandwich structure…. The Examiner's attention is particularly directed to Reference (18) to LeComber et al. which appears to disclose the use of a silicon nitride layer as a gate insulating layer." (Motion at 12). "Thus, having a single reference showing silicon nitride in combination with the intrinsic amorphous silicon sandwiching structure is not material, given that the combination is clearly

[74] Mot. for Reconsideration at 11, 13.
[75] Appeal Brief (Sept. 22, 1999) at 13 (SAMS00768958); Amendment (July 8, 1997) at 8 ('463 prosecution history) (SAMS00768864).
[76] *See also,* '463 File History, Amendment at 5-10 (July 8, 1997); Rule 132 Declaration of Yamazaki at 1-4, Appendices B-E (April 10, 1997) (SAMS000768830-43); Office Action at 2 (Jan. 8, 1997); Office Action at 2 (Oct. 20, 1997); Examiner Interview Summary Record (April 23, 1998); Amendment at 6-14 (May 6, 1998); Office Action at 2 (Jan. 14, 1999); Response at 1-3 (January 20, 1999); Appeal Brief (Sept. 21, 1999); Examiner's Answer (Dec. 1, 1999), Decision on Appeal (May 27, 2004); Revised Motion for Reconsideration and supporting exhibits.

added)). "[T]he Examiner simply states it would be obvious to use the silicon nitride layer of LeComber in that device without providing a sufficient showing that one of ordinary skill in the art would have been motivated to do so. . . . * * * * * Absent any teaching [in LeComber] of the advantages of silicon nitride or any problems from the use of silicon oxide, it is respectfully submitted that one of skill in the art would not, without more, have been motivated to combine LeComber with other references. . . ." (Appeal Br. at 8-9, Sept. 21, 1999). "It is not clear exactly what language in LeComber . . . or other prior art of record the Examiner believes suggests or motivates one of skill in the art to use a SiN [*i.e.*, silicon nitride] gate insulating layer in thin film transistors." (*Id.* at 12) "Also, with respect to LeComber, it is important to note that the type of transistor disclosed by LeComber is entirely different from the transistor disclosed by Matsumura." (*Id.* at p. 13)	taught by other information before the PTO. As noted above, this other information informed the Examiner of the prior art use of silicon nitride as a gate insulator and its known interchangeability with silicon oxide. (Motion at 13). "Silicon oxide can be replaced with silicon nitride as the gate insulator when I consider the paper, P.G. LeComber, Electronics Letters, 'Amorphous Silicon Field Effect Device and Possible Application…" (Motion, Ex. E (Matsumura Decl. at ¶ 6)).

227. Although Dr. Yamazaki has not yet been deposed, Mr. Yamamoto of SEL was substantively involved in the '463 prosecution and conceded that if he were aware of evidence supporting a combination of LeComber's silicon nitride gate insulating layer with Matsumura's TFT, "it's highly likely that it would have been material."[77]

228. In my opinion, Dr. Yamazaki can be charged with the requisite knowledge of the above-described litigation activity and its inconsistency with his prosecution position. First, Dr.

[77] Deposition of Kunitaka Yamamoto ("Yamamoto Dep.") Vol. 2 (Nov. 11, 2009) at 200:24-201:8.

Yamazaki was deposed during the *SEL I* litigation regarding the '636 Patent[78] and disclosed the Motion for Reconsideration and/or the Matsumura Declaration in at least ten other patent applications, including U.S. Patent Nos.: 6,028,264, 6,680,486, 6,346,716, 6,503,771, 7,038,238, 6,660,574, 6,221,701, 6,734,499, 6,043,105, and 6,664,556. Second, throughout the time of the *SEL I* litigation and the prosecution of the '636 and '463 Patents, Dr. Yamazaki was the president and majority shareholder of SEL[79] and he was responsible for coordinating the *SEL I* litigation.[80] Third, Dr. Yamazaki is a named inventor of both the '636 and '463 Patents and exercised significant control over the formulating and approving of patent applications.[81] In fact, the district court in the *SEL I* litigation specifically noted the control that Dr. Yamazaki exercised over patent decisions, stating "[t]here is no doubt…that it is Dr. Yamazaki who ultimately determines what information is disclosed to the PTO in connection with his patent applications." *SEL I*, 4 F. Supp. 2d at 488 n. 18 (noting that Dr. Yamazaki revoked the power of attorney in connection with a patent application because the patent attorney wished to disclose additional references to the USPTO against Dr. Yamazaki's request.) Fourth, although Dr. Yamazaki has not been deposed yet in this case, Mr. Yamamoto of SEL gave testimony suggesting Dr. Yamazaki was involved in the prosecution.[82]

[78] *See e.g.*, Deposition of Dr. Shunpei Yamazaki ("Yamazaki Dep.") Vol. 5 at 659:7-17, 719:7-723:6, 731:5-735:1 (SAMS00766506, SAMS00766566-70, SAMS00766578-82); Yamazaki Dep. Vol. 6 at 777:9-24, 782:10-783:4, 844:20-845:2 (SAMS00766625, SAMS00766630-31, SAMS00766692-93); Yamazaki Dep. Vol. 10 at 1345:24-1347:25, 1373:26-1376:6 (SAMS00767195-196, SAMS00767223-767226).
[79] *SEL I*, 4 F. Supp. at 479.
[80] Declaration of Shunpei Yamazaki ("Yamazaki Decl.") filed in the *SEL I* litigation dated December 3, 1995 ¶ 11 (SAMS00906481-487).
[81] *See* U.S. Patent Nos. '463 and '636; *SEL I*, 4 F. Supp. 2d at 488 n. 18.
[82] Yamamoto Dep. Vol. 3 (November 12, 2009) at 339:1-15.

229. I further understand that Samsung's technical expert, Dr. Fair, is of the opinion that the above-described litigation activity was not cumulative of information of record in the '463 Patent.

230. Further, USPTO policy states that the existence of litigation involving the subject matter for which a patent is sought, and any other material information arising from the litigation, must be brought to the attention of the USPTO.[83]

231. I may opine that Dr. Yamazaki did not call to the attention of the USPTO the existence of the litigation over the '636 Patent to the extent required. While Dr. Yamazaki submitted several copies of the ultimate court decisions (holding that he had committed inequitable conduct in obtaining the '636 Patent), they were submitted only as attachments to documents from a *different* litigation over a *different* patent, and among more than one hundred (100) other items. I may opine that Dr. Yamazaki buried this information.

232. In my opinion, Dr. Yamazaki breached his duty of candor and good faith in the '463 application by concealing information from the '636 litigation, including the Motion for Reconsideration and the Matsumura Declaration.

2. Failure to Disclose Material Prior Art

233. In the event it is shown that Dr. Yamazaki knew that certain undisclosed prior art references -- such as United States Patent No. 4,072,974 ("the '974 Patent") -- were likely to be important to a reasonable examiner, and he is unable to provide a reasonable explanation otherwise during his upcoming deposition, it is my opinion that he failed to meet his duty of disclosure to the USPTO.

234. I understand from Samsung's technical expert, Dr. Fair, that the '974 Patent discloses a thin-film transistor comprising a pair of source and drain regions with an impurity

conductivity type, a channel region between the source and drain regions, a gate electrode adjacent to the channel region, and a portion of a gate insulating film which is in direct contact with the channel region comprises a nitride. The thin-film transistor claimed by independent Claims 1, 5, 8, and 12-14 of the '463 Patent also includes these same limitations.

235. Additionally, I understand that column 4 of the '974 Patent incorporates by reference the teachings of Kemlage (United States Patent No. 3,698,947), which discloses hydrogenation of silicon. Similarly, independent Claims 1, 5, 8, and 12-14 of the '463 Patent each include the hydrogenation of silicon.

236. During prosecution of the '463 Patent, SEL argued that one of the primary reasons the claimed subject matter was patentable over prior art was because of its claim limitations directed to a nitride gate insulating film over the channel, source, and drain regions that were all made from silicon.[84] I understand from Samsung's technical expert, Dr. Fair, that such arguments were inconsistent with the disclosure of the '974 Patent and could not reasonably have been made had the '974 Patent been disclosed. I further understand that the '974 Patent was not cumulative because unlike any other single reference of record, it disclosed a nitride gate insulating film over the channel, source, and drain regions that were all made from silicon, wherein the silicon is hydrogenated.

237. Pending any explanation that Dr. Yamazaki offers at his deposition for these inconsistencies, there is evidence that his failure to disclose the '974 Patent to the USPTO during prosecution of the '463 Patent was done deliberately with knowledge of its materiality. First, Dr. Yamazaki and his company disclosed the '974 Patent to the USPTO in at least nine other SEL patents that issued before the date the '463 Patent was filed, including U.S. Patent Nos.

[83] MPEP § 2001.06(c).
[84] *See e.g.*, SEL's Amendments and Response to Office Action (Jul. 8, 1997) (SAMS00768857-

4,727,044, 5,315,132, 5,313,077, 5,543,636, 6,734,499, 6,635,520, 6,680,486, and 6,221,701. Second, Dr. Yamazaki was also a named inventor on each of those prior patents.[85] Finally, the '974 Patent was also brought to the attention of Dr. Yamazaki and SEL during prosecution of the '132 Patent, on which Dr. Yamazaki is also a named inventor. On March 9, 1993, during the prosecution of the '132 Patent, the examiner rejected the pending claims of the '132 Patent based, in part, on the '974 Patent, and specifically directed Dr. Yamazaki to the '974 Patent's material teachings.[86] Specifically, the examiner remarked that the '132 Patent disclosed a thin-film transistor with polycrystalline source, drain, and channel regions.[87] The examiner also indicated that the '974 Patent disclosed a thin-film transistor that included a channel region of a first conductivity type, source and drain regions of an opposite conductivity type formed on either side of the channel region, a gate insulating layer over the channel, source, and drain regions, and a gate electrode over the gate insulating layer.[88]

238. Further, the '974 Patent was of record in the '636 prosecution history file. However, Dr. Yamazaki disclosed only "selected portions" of that file to the '463 examiner, notably omitting the '974 Patent from those portions of the '636 file history provided to the examiner.

239. Mr. Yamamoto, who worked at SEL and was substantively involved in the '636 and '463 prosecutions, gave testimony in a different litigation suggesting that they basically did

66).

[85] *See* U.S. Patent Nos. 4,727,044, 5,315,132, 5,313,077, 5,543,636, 6,734,499, 6,635,520, 6,680,486, and 6,221,701.

[86] Office Action (March 9, 1993) ('132 Patent file history).

[87] *Id*.

[88] *Id.*

not track information from other patent applications that were related to the same area of technology but not directly related.[89]

240. Based on this information, I may testify that Dr. Yamazaki breached his duty of candor and good faith by failing to disclose the '974 Patent to the examiner for consideration in the '463 patent application.

3. Dr. Yamazaki's Inequitable Conduct in the '636 Patent Had a Necessary and Immediate Relationship With the '463 Patent

241. As described above, the district court and the Federal Circuit in the *SEL I* litigation found that inequitable conduct was committed in obtaining the '636 Patent. I have been asked to determine whether Dr. Yamazaki's inequitable conduct related to the '636 Patent had a necessary and immediate relationship with the '463 Patent in suit. As discussed below, I conclude that it did.

a. The '463 Patent Recaptured Subject Matter of the Unenforceable '636 Patent

242. The district court in the *SEL I* litigation held that Dr. Yamazaki, with intent to deceive, intentionally withheld Japanese Laid-Open Application No. 56-135968 ("the '968 Japanese Application"), even though SEL had submitted the reference to the USPTO, because of the misleading manner in which SEL submitted the reference.[90] In particular, SEL submitted only a partial translation and a concise explanation of the '968 Japanese Application that omitted key material teachings of the reference.[91] The district court also found that SEL had intentionally misrepresented the materiality of a 1983 article by C. C. Tsai, entitled *Amorphous Si Prepared in a UHV Plasma Deposition System*, by characterizing the article as applying

[89] Deposition of Kunitaka Yamamoto (dated 11/30/06) at 59.
[90] *SEL I*, 4 F. Supp. 2d at 484.
[91] *Id*.

primarily to solar cells rather than TFTs.[92] Thus, SEL mislead the examiner into believing that the Tsai article was not material.[93]

243. I understand from Samsung's technical expert, Dr. Fair, that the '636 and '463 Patents share the same subject matter and substantially similar claims. Both patents disclose a thin-film transistor comprising a non-single crystal semiconductor material containing hydrogen or a halogen and having an intrinsic conductivity type. *See e.g.*, '463 Patent Claims 1, 2, 5, 8, 9, 12-14; '636 Patent Claims 4, 5, 7. Additionally, both patents disclose the same thin-film transistor structure wherein the channel region is sandwiched between a silicon nitride gate insulator and another insulator. *See e.g.*, '463 Patent Claims 12-14; '636 Patent Claims 1-5.

244. I further understand that the '463 and '636 Patents claim patentably indistinct subject matter. For example, in the chart below, the corresponding limitations of Claims 1 and 2 of the '463 Patent are compared to the limitations in Claim 4 of the '636 Patent:

'463 Patent Claims 1 and 2	**Corresponding Elements in Claim 4 of the '636 Patent**
1. A thin film transistor comprising:	"A thin film transistor comprising:"
a pair of source and drain regions;	"source and drain regions"
a channel region between said source and drain regions; and	"where the channel region is disposed between the source and drain regions"
N/A	"wherein at least a portion of said channel region contains nitrogen in an amount not exceeding $5x10^{18}$ atoms/cm^3"
a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;	"a gate insulating film comprising silicon nitride directly contacting said channel region; and a gate electrode contacting said gate insulating film"
said channel region comprising an amorphous	"a non-single crystalline semiconductor layer

[92] *Id.* at 486.
[93] *Id.*

silicon semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;	doped with a hydrogen or halogen . . . and having a channel region disposed in the semiconductor layer"
said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof,	"a non-single crystalline semiconductor layer doped with a hydrogen or halogen . . . and having a channel region disposed in the semiconductor layer . . .; source and drain regions forming respective junctions with said channel region"
and having an impurity conductivity type to form junctions in contact with said channel region,	"source and drain regions forming respective junctions with said channel region"
Wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprises a nitride.	"a gate insulating film comprising silicon nitride directly contacting said channel region"
2. A thin film transistor according to claim 1 wherein said channel region has an intrinsic conductivity type.	"a non-single crystalline semiconductor layer . . . having an intrinsic conductivity type and having a channel region disposed in the semiconductor layer"

245. By continuing to seek the '463 claims after the '636 Patent was held unenforceable, SEL essentially recaptured in the '463 Patent certain subject matter of the claims rendered unenforceable in the '636 Patent.

246. For example, Claim 4 of the unenforceable '636 Patent recited a thin film transistor with a non-single crystalline semiconductor material and SEL has argued that one type of such material defined in the '636 Patent is the amorphous silicon semiconductor material recited in Claims 1 and 2 of the '463 Patent.

247. Unenforceable Claim 4 of the '636 Patent further recited certain impurity levels. I understand that the thin film transistors defined in Claim 2 of the '463 Patent could have those impurity levels. I understand from Samsung's technical expert, Dr. Fair, that those levels would

have been common knowledge, especially in light of the Tsai and Canon references that Dr. Yamazaki misrepresented to the USPTO.[94] I further understand that a thin film transistor consistent with Claim 2 of the '463 Patent could well have those impurity levels, and that employing those nitrogen impurity levels would have been well known, especially in light of the Tsai and Canon references that Dr. Yamazaki misrepresented to the USPTO.[95]

248. The common subject matter defined above was encompassed by the '636 Patent and was then recaptured in the '463 Patent after the '636 Patent was held unenforceable by the courts. Indeed, a transistor with the overlapping elements, as shown in the chart above, would equally infringe both patents.

249. Dr. Yamazaki knew of the relationship between the claims in the '463 and '636 Patents at the time he was prosecuting the '463 Patent. During prosecution of the '636 Patent and U.S. Patent No. 6,355,941 ("the '941 Patent"), Dr. Yamazaki cross-referred to both the '636 and '941 Patents multiple times in their file histories during their prosecution. *See e.g.,* '941 Patent File History, Amendment (Jun. 22, 1995) at pp. 4690, 4696; '636 Patent file history, Preliminary Amendment (Jun. 7, 1995) at pp. 74-79 (directing the examiner's attention to the '941 Patent filed on "essentially the same date" as the '636 Patent and which "also include claim subject matter directed to use of silicon nitride as a gate insulating layer"); '636 Patent file history, Supplemental Information Disclosure Statement (Aug. 11, 1995), at p. 80. Notably, the '941 and '463 Patents are in the same family. As detailed above, both patents are continuations of the '102 Application, which issued as the '334 Patent. Further, I understand that SEL

[94] *SEL I,* 4 F. Supp. 2d at 483-486.
[95] *Id.*

contends that the '941 Patent and asserted claims of the '463 Patent are entitled to the priority of the '418, '767, '705 and '102 Applications.[96]

b. Dr. Yamazaki Gained an Advantage in the '463 Patent Prosecution From The Inequitable Conduct He Committed in Obtaining the '636 Claims

250. Dr. Yamazaki committed inequitable conduct in obtaining the '636 Patent by misdirecting the examiner away from untranslated portions of the Canon reference which contained an express suggestion to employ teachings "to reduce carbon, oxygen and nitrogen impurities below the levels claimed in the '636 Patent."[97]

251. Dr. Yamazaki continued and furthered that scheme when he sought and obtained a Certificate of Correction revising the claims of the '636 Patent.

252. In particular, on September 27, 1996, Dr. Yamazaki, through his attorney Mr. Ferguson, alleged that issued Claim 10 of the '636 Patent could be changed through a Certificate of Correction because the correction would be consistent with the recitations in Claims 6-9 and issued Claim 7 already recited the specific levels of carbon, oxygen and nitrogen impurities and had been fully examined:

> Moreover, 37 CFR 1.323 states that the Commissioner may issue the Certificate of Correction if the correction does not involve such changes in the patent as would constitute new matter or would require re-examination. Clearly, the correction does not constitute new matter inasmuch as the corrected recitation is supported at least at page 16, lines 9-12 of the application specification (column 6, lines 9-12 of the patent specification) and, of course, is consistent with present claims 6-9 of the patent.
>
> Moreover, issuance of the Certificate of Correction will not require reexamination of the patent inasmuch as the scope of claim 7, for example, is broader than that of corrected claim 10, where claim 7 recites a concentration of oxygen, carbon or nitrogen in at least a portion of the channel region is not higher than $5x10^{18}$ atoms/cm^3

[96] *See* SEL's Responses to Defendants' First Set of Interrogatories at p. 5; '941 Patent.
[97] *SEL I*, 4. F. Supp. 2d at 483.

> while claim 10 simply recites the carbon concentration in at least a portion of the channel region does not exceed $5x10^{18}$ atoms/cm^3.[98]

253. Dr. Yamazaki's reliance on the recitations in Claims 6-9 and of the impurity levels in Claim 7 was important in obtaining revised Claim 10 through a Certificate of Correction. If Dr. Yamazaki had been unable to convince the USPTO that the Certificate would not materially change the scope of the '636 claims, the Certificate would not issue.[99]

254. I understand from Samsung's technical expert that the recitation of Claim 10 as prosecuted was not unreasonable and is in fact consistent with transistor technology currently in existence. Based on my experience, patent examiners rely on applicants to draft their claims to claim what they believe to be their inventions, and examiners generally will prosecute the claims of a patent application as drafted, so long as the claims are not unreasonable.

255. Additionally, Dr. Yamazaki's reliance on the original examination of Claim 7 was important in obtaining the Certificate of Correction in another way as well. Dr. Yamazaki suggested that since Claim 7 was patentable, so too was corrected Claim 10: "issuance of the Certificate of Correction will not require reexamination of the patent inasmuch as the scope of claim 7, for example, is broader than that of corrected claim 10."[100] In other words, Dr. Yamazaki's Request for Certificate of Correction of the '636 Patent relied on the proposition that Claim 7 was patentable.[101]

256. But, while his Request for Certificate of Correction for the '636 Patent was pending, and unbeknownst to the USPTO, Dr. Yamazaki submitted claims in his '463 Patent

[98] Request for Certificate of Correction (September 27, 1996) at 2 ('636 Prosecution History).
[99] MPEP § 1481 (Sixth Ed., Rev. 2, July 1996, at 1400-64).
[100] Request for Certificate of Correction (September 27, 1996) at 2 ('636 Prosecution History).
[101] Additionally, Dr. Yamazaki's Request implicitly relied on the propriety of Claim 7 when correcting antecedent basis in Claims 1-5: "claims 6-10 already recited the antecedent basis for the term "substrate", these claims, of course, having also already been examined." Request for Certificate of Correction (September 27, 1996) at 4 ('636 Prosecution History).

Application that were patentably indistinct from Claim 7 of the '636 Patent. For example, Claims 85 and 86 of the '463 Patent Application were added by amendment on July 10, 2007, and read as follows:

> 85. A thin film transistor comprising:
>
> a pair of source and drain regions;
>
> a channel region between said source and drain regions; and
>
> a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;
>
> said channel region comprising an intrinsic non-single semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof;
>
> said pair of source and drain regions comprising a non-single crystal semiconductor material doped with a recombination center neutralizer selected from the group consisting of H, a halogen and a combination thereof, and having a P or N type conductivity to form PI or NI junctions in contact with said channel region,
>
> wherein at least a portion of said gate insulating film which is in direct contact with said channel region comprises a nitride.[102]

257. The proposed correction to Claim 10 of the '636 patent would make it more like Claim 86 of the pending '463 Patent Application. I understand from Samsung's technical expert that proposed Claim 10 would have been obvious over the invention recited in Claim 86 of the '463 Patent Application in light of other known prior art such as Tsai and Canon. In my opinion, Dr. Yamazaki should have disclosed the '463 Patent Application before the USPTO granted his request to revise Claim 10 of the '636 Patent. Instead, further to his deceitful misrepresentation of Tsai and Canon, Dr. Yamazaki withheld entirely the '463 Patent Application in the '636 proceedings.

[102] Amendment (July 10, 1997) at 1-2 ('463 Prosecution History) (SAMS00768858-59).

258. Dr. Yamazaki's requested Certificate of Correction issued on August 6, 1996, thereby revising Claim 10 of the '636 Patent without the USPTO. But, Dr. Yamazaki never told the USPTO about the Canon or Tsai references, or about the '463 Patent Application.[103] In my opinion, this was in furtherance of the inequitable conduct he committed in obtaining the original '636 Patent.

259. If Dr. Yamazaki had properly revealed Canon, Tsai, and the '463 Patent Application while obtaining the '636 Certificate of Correction, the USPTO would have been alerted to the double patenting issue between the '636 Patent and the '463 claims. I understand from Samsung's technical expert that revised Claim 10 of the '636 Patent, in combination with other known art such as the Canon and Tsai references, would have established at least a *prima facie* case of unpatentability against one or more of the '463 claims pending during the Certificate of Correction Proceedings and one or more of the issued '463 claims. In my opinion, Dr. Yamazaki deceived the USPTO into issuing the '463 Patent without entering such a rejection. That was an advantage Dr. Yamazaki gained in the '463 Patent Application from the inequitable conduct he committed in connection with the '636 Patent.

260. Dr. Yamazaki knew that the '463 Patent could have obviousness-type double patenting problems. For example, in the '463 prosecution history, Dr. Yamazaki received a provisional double patenting rejection over an application (S.N. 470,599) directed to subject matter related to the '636 Patent.[104] Indeed, Dr. Yamazaki, through his attorney Mr. Ferguson, acknowledged that the '636 Patent was directed to subject matter related to the '599

[103] Request for Certificate of Correction (September 27, 1996) at 1 ('636 Prosecution History).
[104] Office Action (January 29, 1996) at 2 ('463 Prosecution History) (SAMS00768088-8089); *see also*, Office Action (March 5, 1992) at 2 ('463 Prosecution History) (obviousness-type double patenting rejection over Dr. Yamazaki's U.S. Patent No. 4,581,620) (SAMS00767937).

Application.[105] The provisional rejection should have alerted Dr. Yamazaki to the double patenting issue between the '463 Patent and the '636 Patent.

261. By continuing to rely on the original, tainted examination of Claim 7, the Request For Certificate of Correction was presented in violation of 37 CFR § 11.18(b)(1). That section mirrors Rule 56 by prohibiting later advocating a paper that willfully covers up a material fact by any trick, scheme or device. In his Request for Certificate of Correction, Dr. Yamazaki advocated a paper (the '636 Patent prosecution history and allowance of Claim 7) that willfully covered up a material fact (the impurity disclosures in Canon) by a trick, scheme, or device (submitting a misleading concise statement of Canon's relevance) in violation of Rule 56.

262. Such a violation of 37 CFR § 11.18(b)(1) may jeopardize the enforceability of any resulting patent.[106] The '463 Patent may be considered a "resulting patent" at least to the extent that it otherwise would not have issued in its current form (without a terminal disclaimer).

263. Dr. Yamazaki further ensured that the examiner of the '463 Patent would not be alerted to the double patenting issue with the '636 Patent by burying the '636 Patent in a huge volume of materials dumped on the '463 examiner. In fact, the IDS submitted on October 8, 2003, which included the '636 Patent references, consisted of 135 references (including numerous pleadings, articles, and other materials). Overall, the file history and references submitted to the USPTO for the '463 Patent was approximately 4500 pages, which included 328 separate references.

264. Burying information submitted to the USPTO can be considered a violation of the duty of disclosure.[107] Thus, the USPTO advises applicants to avoid such burying:

[105] Supplemental Information Disclosure Statement (August 11, 1995) at 1 ('636 Prosecution History).
[106] 37 CFR § 10.18(c) (2001).
[107] MPEP § 2002.03 (Fifth Ed., Rev. 3, May 1986, at 2000-8).

> 13. It is desirable to avoid the submission of long lists of documents if it can be avoided. Eliminate clearly irrelevant and marginally pertinent cumulative information. If a long list is submitted, highlight those documents which have been specifically brought to applicant's attention and/or are known to be of most significance. See *Penn Yan Boats, Inc. v. Sea Lark Boats, Inc.*, 359 F. Supp. 948, 175 USPQ 260 (S.D. Fla. 1972), *aff 'd*, 479 F.2d 1338, 178 USPQ 577 (5th Cir. 1973), *cert. denied*, 414 U.S. 874 (1974). But cf. *Molins PLC v. Textron Inc*., 48 F.3d 1172, 33 USPQ2d 1823 (Fed. Cir. 1995).[108]

265. In the '463 prosecution, Dr. Yamazaki presented the '636 Patent only as an attachment to the Declarations of Peter J. Wied and Donald R. Harris, which were themselves attachments to motions among a long list of materials from litigation with Acer concerning the '941 Patent.[109] And, the motions concerned inequitable conduct and not double patenting.[110] In contravention of the USPTO's advice discussed above, Dr. Yamazaki did not highlight those documents (e.g. the '636 Patent) from the list that were known to be of most significance.[111] Dr. Yamazaki clearly knew how to highlight documents selected from a long IDS list, as he did so on several occasions.[112]

266. Dr. Yamazaki, through his attorney Mr. Robinson, specifically misdirected the attention of the '463 examiner away from material aspects (e.g. double patenting) of the '636 Patent by telling the USPTO that "[a]pplicants are merely making these documents available to the Patent Office as a result of the contentions of the parties in the referenced [Acer]

[108] MPEP § 2004 (Eighth Ed., Rev. 1, February 2003, at 2000-10).
[109] *See* Declaration of Peter J. Wied in Support of Acer Incorporated and Acer America Corporation's Motion for Summary Judgment of Unenforceability of U.S. Patent No. 6,353,941 (SAMS00769344-50); Declaration of Donald R. Harris in Support of SEL's Opposition to Five Summary Judgment Motions of AU and Acer (SAMS0076890).
[110] *Id.*
[111] MPEP § 2004 (Eighth Ed., Rev. 1, February 2003, at 2000-10).
[112] *See e.g.*, Information Disclosure Statement (July 8, 1997) (SAMS00768846-47); Information Disclosure Statement (July 13, 1999) (SAMS00768937-38); Information Disclosure Statement (March 3, 2003) (SAMS00769151-53).

litigation."[113] The contentions of the parties in the Acer litigation, however, did not relate to the material double-patenting aspect of the '636 claims.

267. In my experience in working with examiners and in examining applications as an Examiner-in-Chief, there is very little chance that the examiner would even look at the '636 claims in response to such a submission because examiners do not examine patent applications for possible inequitable conduct. The examiner would not have been prompted to consider the '636 Patent at all in response to Dr. Yamazaki's statement of its relevance ("merely…. as a result of the contentions of the parties in the referenced litigation").

268. That misdirection is comparable to the inequitable conduct Dr. Yamazaki employed by submitting to the '636 examiner a concise explanation of the Canon reference that misdirected the USPTO away from the material portions of the Canon reference:

> By submitting the entire untranslated Canon reference to the PTO along with a one-page, partial translation focusing on less material portions and a concise statement directed to these less material portions, ***SEL left the examiner with the impression that the examiner did not need to conduct any further*** *translation or* ***investigation***. Thus, SEL deliberately deceived the examiner into thinking that the Canon reference was less relevant than it really was, and constructively withheld the reference from the PTO. SEL's submission hardly satisfies the duty of candor required of every applicant before the PTO.
>
> * * * *
>
> The duty of candor does not require that the applicant translate every foreign reference, but only that the applicant refrain from submitting partial translations and concise ***explanations that it knows will misdirect the examiner's attention from the reference's relevant teaching.***[114]

269. Thus, the misdirection Dr. Yamazaki employed in avoiding a double patenting rejection and obtaining the '463 Patent appears to be part of an established pattern of misconduct

[113] Information Disclosure Statement and Notice of Litigation under MPEP 2001.06(C) (October 8, 2003) at 3 ('463 prosecution history) (SAMS00769338).

aimed at misdirecting the USPTO away from material portions of references that may be of record. Indeed, Dr. Yamazaki's successful misdirection of the '463 examiner away from the materiality of the '636 Patent appears to be in furtherance of "a sophisticated, subtle, and consistent effort to hide the ball from the USPTO in a manner plainly at odds with an applicant's duty of candor, good faith, and honesty."[115] Dr. Yamazaki's "consistent effort" occurred during the '636 prosecution and continued through the '463 prosecution.

270. As reflected on the face of the '463 Patent, the USPTO considered the '636 Patent only in connection with the Acer litigation materials.[116]

271. I understand that Samsung's technical expert, Dr. Fair, is of the opinion that, due to obviousness-type double patenting, the '636 Patent was highly material to patentability of at least one claim of the '463 Patent.

272. While the '463 examiner issued obviousness-type double patenting rejections over patents that were properly disclosed,[117] he did not raise the double patenting issue with respect to the '636 Patent.

273. In my opinion, Dr. Yamazaki's successful burying of the '636 Patent and his misdirection and misleading explanation of why it was being submitted was a violation of his duty of candor and good faith in obtaining the '463 Patent.

274. Dr. Yamazaki's inequitable conduct in obtaining the '636 Patent, and the resultant Acer litigation materials, thus provided Dr. Yamazaki with the perfect cover for burying the '636

[114] *SEL*, 204 F.3d at 1377-78 (emphasis added).
[115] *SEL*, 204 F.3d at 1373 (*quoting SEL v. Samsung*, 4 F. Supp 2d 477, 496 (E.D. Va. 1998).
[116] *See* '463 Patent, page 6; *see also* form 1449, initialed 11/03 (SAMS00769345).
[117] *See e.g.*, Office Action (August 13, 1991) (SAMS00767849); Office Action (March 5, 1992) (SAMS00767938); Office Action (May 9, 1994) (SAMS00768037); Office Action (June 2, 1995) (SAMS00768071-72); Office Action (January 29, 1996) (SAMS00768089); Office Action (July 11, 1996) (SAMS00768104).

Patent and misdirecting the examiner away from its materiality during the '463 prosecution.[118] This was an additional advantage Dr. Yamazaki attained in the '463 prosecution as a result of obtaining the '636 Patent through inequitable conduct

(1) One-way Versus Two-way Obviousness-type Double Patenting

275. I understand from Samsung's technical expert that corrected Claim 10 of the '636 Patent would have rendered the subject matter of at least one claim of the issued '463 Patent *prima facie* obvious. Indeed, I understand from Samsung's technical expert that at least one claim of the issued '463 Patent is invalid for two-way double patenting over the invention claimed in the corrected '636 Patent. At the very least, the corrected '636 Patent in combination with other information known to Dr. Yamazaki (such as the Canon and Tsai references discussed in *SEL I*) would have created a *prima facie* case of one-way obviousness-type double patenting against at least one claim of the '463 Patent.

276. In my opinion, one-way obviousness is all that is necessary to reject the '463 Patent claims as an obvious variation of the invention claimed in the corrected '636 Patent. In applying USPTO procedures to determine whether one-way or two-way obviousness is necessary, one might consider whether (in light of their effective filing dates) the '463 Patent Application was filed earlier than the '636 Patent Application. I have not evaluated the effective filing dates, but I note that the '463 Patent has a later issue date than the '636 Patent.

277. Even assuming the '463 Patent Application is treated as having been filed earlier, two-way obviousness is not required because its later issue date was not a result of administrative delay but rather the control Dr. Yamazaki exerted over the prosecution timing. The issued '463

[118] Information Disclosure Statement and Notice of Litigation under MPEP 2001.06(C) (October 8, 2003) at 3 ('463 prosecution history) ("[a]pplicants are merely making these documents available to the Patent Office as a result of the contentions of the parties in the referenced [Acer]

claims were not presented to the USPTO in their current form until after the ‘636 Patent had already issued. I understand that the claims pending before that time in the ‘463 Patent Application were directed to various other inventions.

278. Had Dr. Yamazaki timely presented claims to the subject matter covered by the ‘463 Patent, he would have been under a duty to disclose that fact to the examiner of the ‘636 Patent Application because it was material to patentability of the ‘636 claims. And, had he done so, the USPTO should have issued a double patenting rejection in both the ‘463 and ‘636 Patent Applications.

279. I am not aware of any reason Dr. Yamazaki could not have presented the ‘463 claims in the ‘636 Patent Application just as easily as he presented them in the ‘463 Patent Application.

280. If the ‘463 Patent is credited with the asserted effective filing date of 1981 or earlier, Dr. Yamazaki could have presented claims to the currently claimed invention of the ’463 Patent in 1981. Instead, he delayed at least fifteen years. Any administrative delay that might be blamed on the USPTO in examining the currently claimed invention is far less than the fifteen-plus year delay introduced voluntarily by Dr. Yamazaki.

281. Thus, only one-way obviousness should be required in evaluating the claims of the ‘463 Patent for obviousness-type double patenting over the invention claimed in the ‘636 Patent.

(2) Nonobviousness-type Double Patenting

282. Even if certain claims of the ‘463 Patent were nonobvious in view of the invention claimed in the ‘636 Patent and vice-versa, such claims could have been rejected for nonobviousness-type double patenting.

litigation”) (SAMS00769338).

283. The ‘463 Patent provided Dr. Yamazaki with an unwarranted time-wise extension of exclusivity over subject matter covered by the ‘636 Patent. The ‘636 Patent issued on August 6, 1996, and claims priority to a U.S. patent application filed on May 20, 1985. Dr. Yamazaki disclaimed any portion of the ‘636 Patent term extending beyond the expiration date of the ‘132 Patent. As indicated on the face of the ‘132 Patent, Dr. Yamazaki disclaimed any portion of the ‘132 Patent term extending beyond September 25, 2007. However, the ‘463 Patent did not receive any double patenting rejections and is not subject to any terminal disclaimer. The ‘463 Patent issued on May 31, 2005, almost nine years after the ‘636 Patent issued.

284. I understand that the claims of the ‘636 Patent and the ‘463 Patent both cover certain common subject matter. For example, I understand that the thin film transistors defined in Claim 2 of the ‘463 Patent are also covered by Claim 4 of the ‘636 Patent if they have the impurity levels recited in Claim 4 (*see* side by side comparison chart in Section VII(A)(3)(a) above).

285. Again, due to Dr. Yamazaki’s inequitable conduct, no such analysis was considered by the USPTO.

(3) Reissue was Required Because the Revision of Claim 10 Changed the Scope and Meaning of the ‘636 Patent

286. Regarding Dr. Yamazaki’s Request for Certificate of Correction of the ‘636 Patent, I understand from Samsung’s technical expert that the proposed correction to Claim 10 materially affected the scope and meaning of the ‘636 Patent. For example, the revision meant that the gate electrode in Claim 10 no longer needed to comprise silicon and nitrogen. Likewise, the revision meant that the gate insulating film in Claim 10 now needed to comprise silicon and nitrogen.

287. In telling the USPTO otherwise in his Request for Certificate of Correction, Dr. Yamazaki relied on the notion that Claim 7 (with its impurity level recitations) had been properly

examined and issued in the initial prosecution of the ‘636 Patent.[119] During the pendency of his Request for Certificate of Correction, Dr. Yamazaki failed to inform the USPTO that he had introduced claims in the ‘463 Patent Application that were patentably indistinct from proposed Claim 10. Dr. Yamazaki also failed to reveal the impurity information that he concealed to obtain Claims 7 and 10 in the first place. In my opinion, Dr. Yamazaki continued his inequitable conduct and did not comport himself with candor and good faith in obtaining the Certificate of Correction.

288. Based on the above understandings, it is my opinion that Dr. Yamazaki should have applied for a reissue patent instead of a Certificate of Correction. In a reissue proceeding, Dr. Yamazaki would have had a duty to disclose all known information material to patentability, such as the co-pending ‘463 claims.[120] Dr. Yamazaki should have been subject to a provisional rejection of at least Claim 10 of the ‘636 Patent for obviousness-type double patenting over the ‘463 Patent Application. In that event, under USPTO procedures the examiner of the ‘463 Patent would have been alerted and would have issued a rejection of the ‘463 claims for double patenting over the invention claimed in the ‘636 Patent.

289. Had Dr. Yamazaki revealed that his change to Claim 10 would change the scope of the ‘636 Patent, and thus been forced into reissue, the ‘463 examiner should have been alerted to the double patenting issue. But, by misrepresenting to the USPTO that there was no change in scope, Dr. Yamazaki avoided reissue and avoided alerting the ‘463 examiner to the double patenting issue. This facilitated obtaining the ‘463 Patent without disclaiming the term extending beyond the expiration date of the ‘636 Patent.

[119] Unbeknownst to the USPTO, that examination was fatally flawed by Dr. Yamazaki’s inequitable conduct and concealment of the impurity level information contained in the prior art.
[120] MPEP § 2003 (Sixth Ed., Rev. 2, July 1996, at 2000-6).

290. Under USPTO policy, a rejection for double patenting entered against the ‘636 claims over the invention claimed in the ‘463 Patent Application would have also been entered against the pending ‘463 claims. Having manipulated the system so as to avoid such a rejection against the ‘636 claims, Dr. Yamazaki managed to avoid alerting the examiner of the ‘463 Patent to the double patenting issue.

B. Suspect Signatures

291. On June 25, 1981, Dr. Nagata and Dr. Yamazaki purportedly executed an Assignment by Joint Inventors agreement, assigning the invention disclosed and claimed in the United States patent application for a “Semiconductor Device” (“1981 Assignment”) to Dr. Yamazaki. The 1981 Assignment was ultimately recorded at the USPTO on June 29, 1981, at Reel 3898, frames 214-215.

292. Also on June 25, 1981, Dr. Yamazaki and Dr. Nagata purportedly executed a Declaration and Power of Attorney (“1981 Declaration”). The 1981 Declaration purported to assign an invention disclosed and claimed in an application for a “Semiconductor Device.” The 1981 Declaration stated that no application for the invention had been filed in a country other than the United States except for Japanese Patent Application No. 88974/80, filed June 30, 1980.

293. On June 29, 1981, U.S. Patent Application No. 06/278,418 was filed in the USPTO, which claimed priority to Japanese Patent Application No. 55-88974 filed June 30, 1980.

294. On October 23, 1990, after a series of continuing applications, U.S. Patent Application No. 07/601,437 (“the ‘437 Application”) was filed.

295. On February 7, 1991, the examiner in the ‘437 Application issued an Office action, rejecting the pending claims under 35 U.S.C. § 102(e) as being anticipated by Yamazaki’s U.S. Patent No. 4,239,554 (“the ‘554 Patent”), which was filed on July 16, 1979 and

issued on December 16, 1980.[121] The Office action quoted § 102(e) in part, as saying that a person shall be entitled to a patent unless "(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant." Under USPTO procedures, the '554 Patent would have been considered to be filed "by another" because the named inventive entity of the '554 Patent (Dr. Yamazaki as a sole inventor) was different than the named inventive entity of the '437 Patent (Dr. Yamazaki and Dr. Nagata as joint inventors).

296. On April 9, 1991, the examiner in the '437 Application held an in-person interview with Dr. Yamazaki, his attorney Mr. Ferguson, Mr. Yanai, and Ms. Nakano. In the Examiner Interview Summary Record, the examiner wrote, in part, that applicant "may change the status of the instant application to a continuation in part of 4,409,134."[122]

297. A continuation-in-part application ("CIP") is a patent application filed during the pendency of another application, repeating some substantial portion or all of the earlier application and adding matter not disclosed in the earlier case. The USPTO permitted an application to be designated a CIP if:

> 1. The first application and the alleged continuation application were filed > with at least one common<** inventor;
>
> 2. The alleged continuing application was "filed before the patenting or abandonment of or termination of proceedings on the first application or an application similarly entitled to the benefit of the filing date of the first application"; and
>
> 3. The alleged continuing application "contains or is amended to contain specific reference to the earlier filed application."[123]

[121] SAMS00767704-14.
[122] SAMS00767716.
[123] MPEP § 201.08 (Fifth Ed., Rev. 11, April 1989 at 200-13).

298. When a string of more than two applications was filed serially, and a later application in the string claimed priority through intervening applications to the first in the string, USPTO policy required appropriate action to be taken in each one of the intervening applications due to the requirement that it be "similarly entitled" to the benefit of the first application filing date.

299. A CIP has a special requirement for its inventor oath or declaration. In addition to the usual requirements, such as acknowledging the Rule 56 duties generally, a CIP declaration must also acknowledge the duty to disclose material information under Rule 56 which occurred after the earlier application but before the CIP:

> (d) In any continuation-in-part application filed under the conditions specified in 35 U.S.C. 120 which discloses and claims subject matter in addition to that disclosed in the prior copending application, the oath or declaration must also state that the person making the oath or declaration acknowledges the duty to disclose material information as defined in § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.[124]

300. Under USPTO policy and procedure, an inventor oath or declaration is inherently material. In my opinion, one important function served by the inventor oath or declaration is to make sure the named inventors formally commit to fulfilling their duties under Rule 56. Another is to have the inventors understand and accept the consequences (fine, imprisonment, and vitiation of the application and of resulting patents) of any false statements and the like. Another is to have a sworn statement from the named inventors as evidence of their belief that they are the original and first inventors of the invention claimed.

301. On May 6, 1991, Dr. Yamazaki, through his attorney Mr. Ferguson, amended his '437 Application to recite that it is "a continuation-in-part of U.S Application No. 237,607 filed

February 24, 1981 (now U.S. Patent 4,409,134 issued October 11, 1983)."[125] He argued that the '437 and '607 Applications had common subject matter and were co-pending. He further argued that "with respect to this common subject matter, the claims of the subject ['437] application are entitled to the February 24, 1981 filing date of the '134 patent."[126] As a result of this CIP priority claim, he argued, the '554 Patent was no longer available as a prior art reference.[127]

302. On August 13, 1991, there was apparently an Office action issued that refused to recognize the CIP priority claim. This Office action is missing from the reconstructed file history I have seen, but is referenced in later documents.[128]

303. On September 30, 1991, Dr. Nagata purportedly executed a Substitute Declaration and Power of Attorney for Patent Application, and an Assignment to SEL, concerning U.S. Patent Application No. 07/488,102.[129] I understand that this is a questioned document. The '102 Application was the parent of the then-pending '437 Application, and ultimately the grandparent of the '264 Application that issued as the '463 Patent-in-suit. The questioned Substitute Declaration claimed priority to the '609 Application and other intervening applications. Importantly, it acknowledged the duty to disclose material information under Rule 56 which occurred between the filing date of the prior application and the filing date of the '102 Application as required to be considered a Continuation-in-Part application ("insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application").

[124] 37 CFR. § 1.63(d) (1989) (the requirement is currently stated in 37 CFR § 1.56(e)).
[125] Amendment (5/2/91) ('463 Patent prosecution history) (SAMS00767717).
[126] Amendment (5/2/91) ('463 Patent prosecution history) (SAMS00767720).
[127] Amendment (5/2/91) ('463 Patent prosecution history).
[128] The USPTO lost portions of the '463 Patent Application prosecution history, and ultimately attempted to reconstruct the file history. *See* Office Action (12/16/04) (SAMS00769448-51).
[129] SEL-SAM0056698-701.

304. On October 21, 1991, Dr. Yamazaki filed an inventor declaration related to the '102 Application.[130] Presumably, this was the questioned "Substitute" declaration discussed above that was purportedly signed by Dr. Nagata on September 30, 1991. In my opinion, the questioned "Substitute" declaration was prepared and submitted to the USPTO in order to overcome the rejection of the '102 Application over Dr. Yamazaki's '554 Patent.

305. On October 30, 1991, it appears that Dr. Yamazaki, through his attorney Mr. Ferguson, faxed a "Preliminary Amendment" for discussion at an upcoming November 7, 1991, interview regarding the '437 Application.[131] The Preliminary Amendment proposed to make the '437 Application a direct CIP of the '609 Application. In my opinion, under USPTO procedures this proposal was improper because the '437 Application (filed October 23, 1990) was never co-pending with the '609 Application (which issued as the '134 Patent on October 11, 1983), despite Dr. Yamazaki's argument that the '437 Application had an "effective" filing date of June 29, 1981.

306. The October 30, 1991, Preliminary Amendment offered a detailed legal argument in support of Dr. Yamazaki's position that "neither the Rules of Practice nor the MPEP require filing reissues and/or amending abandoned intervening applications."[132] Dr. Yamazaki represented that "all intervening applications… prior to the subject application do reference their respective earlier applications up to the first in the string of these applications – that is, the '418 application." The preliminary amendment concluded: "it is urged that the subject application has been properly made a continuation-in-part of application Serial No. 237,609 filed February 24, 1981."

[130] *See* Patent Application and Information Retrieval (PAIR) system electronic records of the USPTO for the '463 Patent.
[131] SAMS00767927-32.
[132] SAMS00767930.

307. On November 7, 1991, an in-person interview was held regarding the '437 Application between the examiner, Dr. Yamazaki, and Mr. Ferguson. According to the Examiner Interview Summary Record, among other things, "Applicant discussed CIP procedures with respect to U.S. 4,409,134." [133]

308. On December 12, 1991, Dr. Yamazaki, through his attorney Mr. Ferguson, filed an Amendment in the '437 application. He acknowledged the November 7, 1991, interview with the examiners and Dr. Yamazaki.[134] The Amendment was said to be in response to the Office action of August 13, 1991, and stated that "[i]in the Office Action, it is stated that applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 120." The Amendment further stated that this issue was discussed with the examiners at the interview.

309. The December 12, 1991, Amendment further stated that although Dr. Yamazaki disagreed with the USPTO's requirement to amend intervening applications, he was doing so nonetheless in order to expedite prosecution. Dr. Yamazaki argued that, as a result, he would be entitled to the filing date of the '609 Application and that the rejection of claims 16-31 over Yamazaki's '554 Patent under 35 U.S.C. § 102(e) should be withdrawn because the '554 Patent "is no longer available as prior art."

310. On December 16, 1991, SEL filed the questioned Assignment of Patent Application or Patent, purporting to record an assignment by Dr. Nagata for a "Semiconductor Device," dated December 11, 1991.

311. On March 5, 1992, the '467 examiner issued an Office action. Among other things, the Office action maintained the rejection over Yamazaki's '554 Patent because the

[133] SAMS00767912.
[134] SAMS00767913-26.

amendments to the string of intervening priority applications had not been completed. In particular, the applicant's request to reissue the '620 Patent and insert the required reference to the '609 application had not yet been granted.

312. On July 29, 1992, Dr. Yamazaki and Mr. Ferguson again met with the examiner concerning the '467 Application.[135] In the Examiner Interview Summary Record, the examiner indicated that the Applicant wanted to amend the claims but that the amendment would not be entered because it was after final rejection.

313. On or around September 8, 1992, Dr. Yamazaki, through his attorney Mr. Ferguson, filed the '264 Application as a continuation of the '467 Application. Thereafter, on or around December 11, 1992, Dr. Yamazaki, through his attorney Mr. Ferguson, filed a Preliminary Amendment in the '264 Application. Among other things, the Preliminary Amendment stated that the required reissue of the '620 Patent had been submitted, and that the rejection over Yamazaki's '554 Patent should be withdrawn as soon as the examiner's requirements were satisfied.[136] The rejection over the '554 Patent was subsequently withdrawn, and after additional rejections were also overcome, the '264 Application eventually issued as the '463 Patent-in-suit.

314. In my opinion, the questioned "Substitute Declaration" filed in the parent '102 Application led directly to issuance of the '463 Patent because it was required in overcoming the rejection over the '554 Patent. But for the questioned "Substitute Declaration," the '463 Patent in suit would not have issued as it did.

[135] SAMS00767963-93.
[136] SAMS00767966.

315. I understand that Dr. Nagata says he did not sign the Assignment and Substitute Declaration and Power of Attorney dated September 30, 1991, and the Assignment dated December 11, 1991.

316. I further understand that Samsung's handwriting expert is of the opinion that it is highly unlikely that the three purported signatures of Dr. Nagata on the documents dated September 30 and December 16, 1991, were signed by Dr. Nagata. I further understand that the handwriting expert believes that the three signatures on the documents from September 30 and December 16, 1991 were likely not written by the same person that signed the documents dated June 25, 1981.

317. Under USPTO regulations, and in my personal experience, knowingly submitting to the USPTO a document with a forged signature is considered a serious violation of the duty of candor and good faith.

318. Thus, to the extent that Dr. Nagata's signature on the "Substitute Declaration" was forged, and Dr. Yamazaki (or any other person substantively involved in the prosecution of the '463 Patent) knowingly prepared or submitted to the USPTO such a forged Declaration, it is my opinion that this constitutes a serious and highly material breach of the duty of candor and good faith.

C. Prosecution Laches

319. The issued claims of the '463 Patent in their current form were not presented to the USPTO in the '463 chain of applications until at least about 1996. It appears that claims pending in the '463 Application chain before that time addressed subject matter different than the issued claims in the '463 Patent. Indeed, Mr. Kunitaka Yamamoto of SEL testified that the

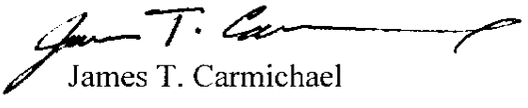
claims of the '463 Patent changed a lot over the years since the original filing of the application in 1981.[137]

320. I understand Samsung may contend that claims of the issued '463 Patent were not necessarily entitled to their asserted effective filing date of 1981 or earlier. However, if the '463 Patent is credited with the asserted effective filing date of 1981 or earlier, Dr. Yamazaki could have presented claims to the currently claimed invention of the '463 Patent in 1981. Instead, he delayed at least 15 years.

321. Based on this information, I may opine that a delay of about fifteen years was unreasonable. I may also opine that such a delay is unexplained from the materials I have considered thus far.[138] Additionally, unless Dr. Yamazaki provides information explaining such a delay at his upcoming deposition, I may opine that it would fit the criteria employed by the USPTO in rejecting applications for prosecution laches.

Dated: December 15, 2009

Respectfully submitted,



James T. Carmichael

[137] Deposition of Kunitaka Yamamoto ("Yamamoto Dep.") Vol. 2 (Nov. 11, 2009), at 135:7-23.
[138] Mr. Yamamoto gave testimony suggesting that in 1996, in conjunction with Dr. Yamazaki, they were attempting to draft claims such that they would cover Samsung. *See* Yamamoto Dep. Vol. 3 (Nov. 12, 2009) at 330:25-338:24.